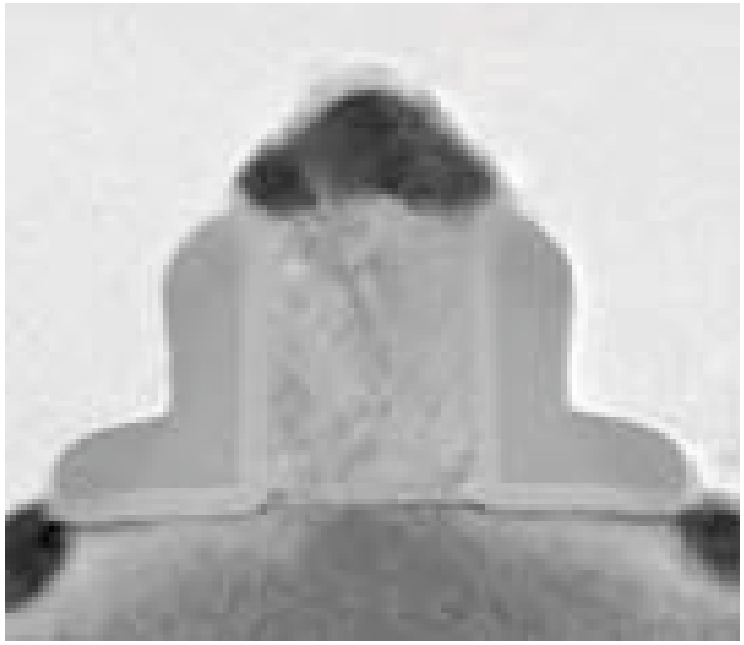
CMOS technology beyond 22nm: Where can silicon take us?

Kelin J. Kuhn
Intel Fellow
Director of Advanced Device Technology
Intel Corporation

Future Challenges in Device Scaling

As near as I can tell: THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size



130 nm

K. Kuhn, MIT 2008

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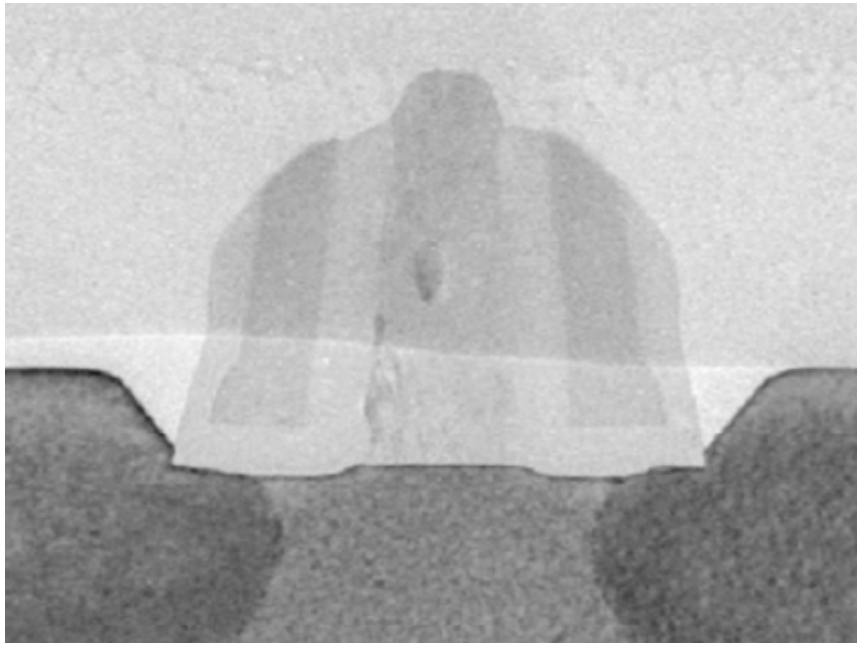

90 nm

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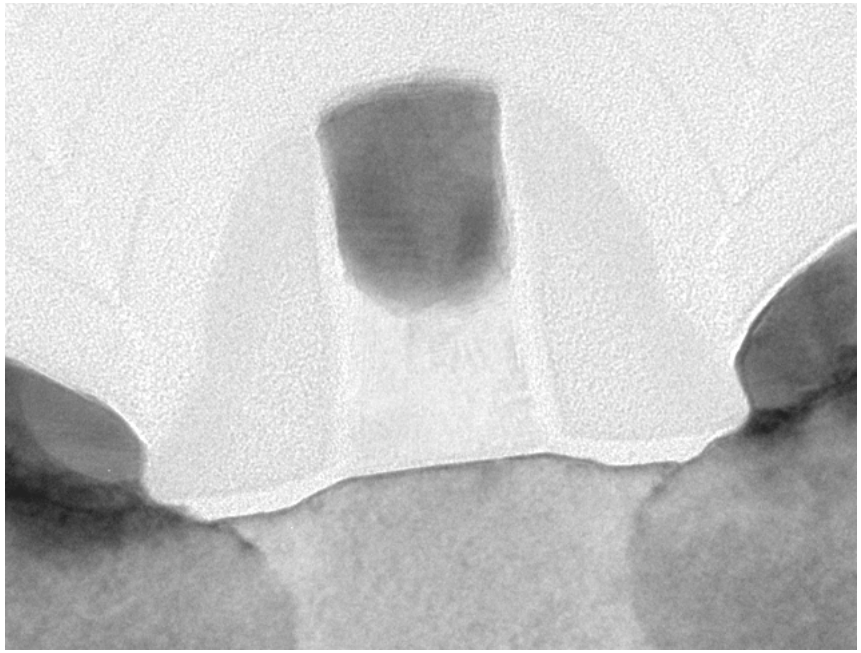

65 nm

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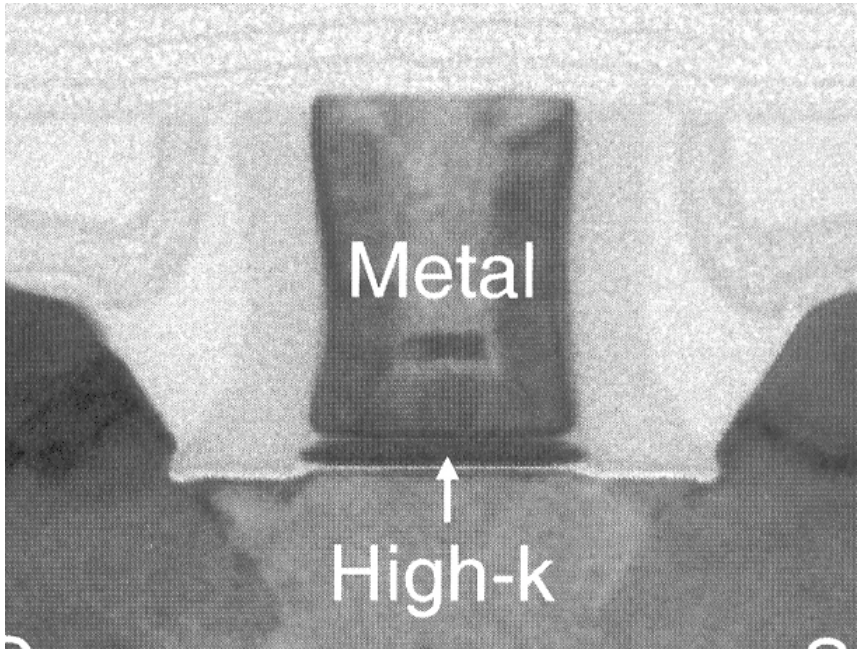

45 nm

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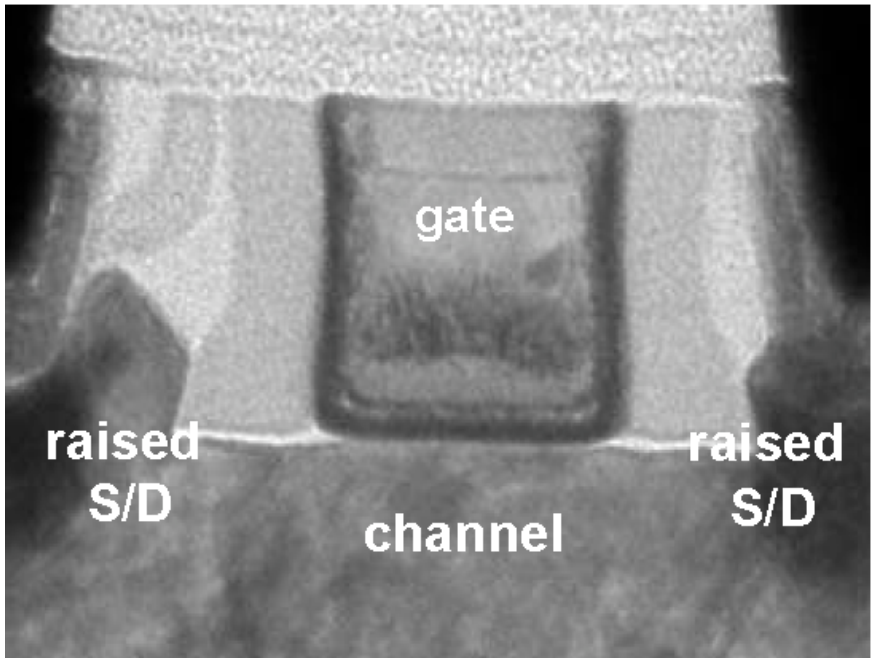

32 nm

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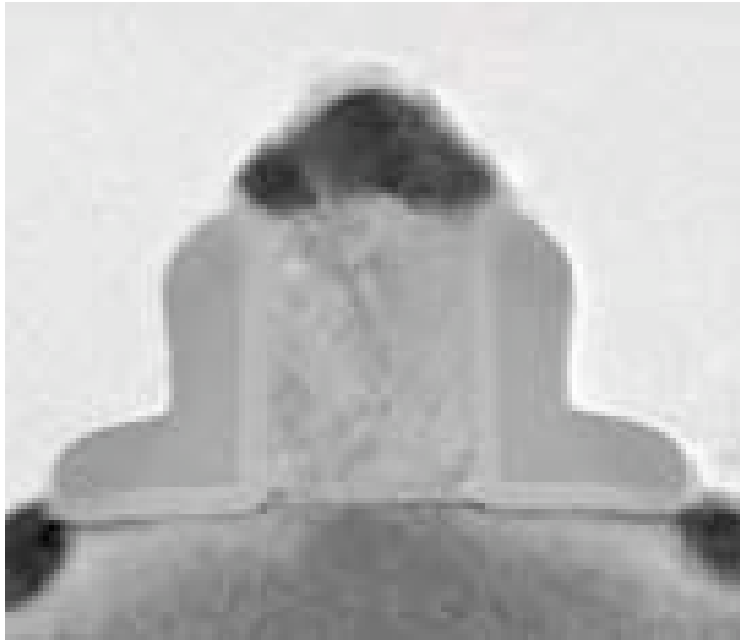

130 nm

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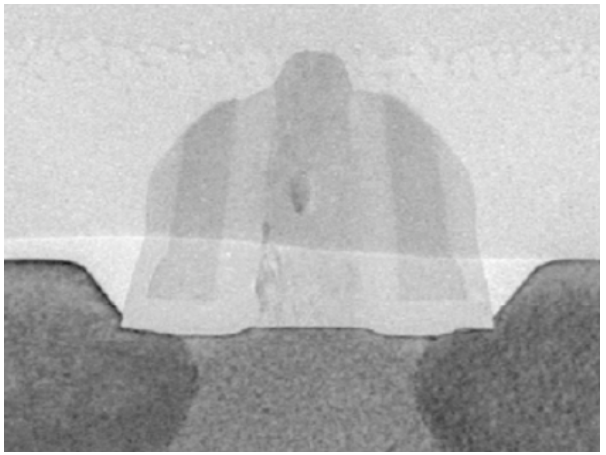

90 nm

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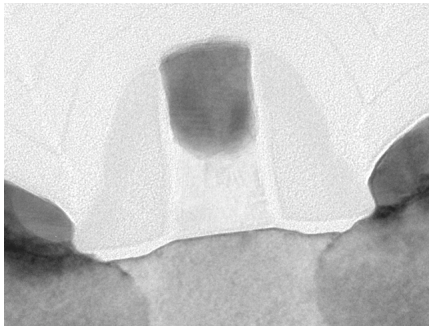

65 nm

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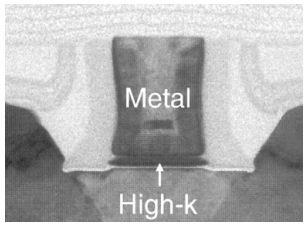

45 nm

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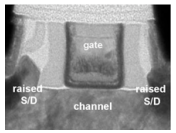

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AGENDA

- Scaling history
- Gate control
  - High-k metal-gate
  - Structural enhancements
- Resistance
- Capacitance
- Mobility
  - Strain
  - Orientation
- Summary

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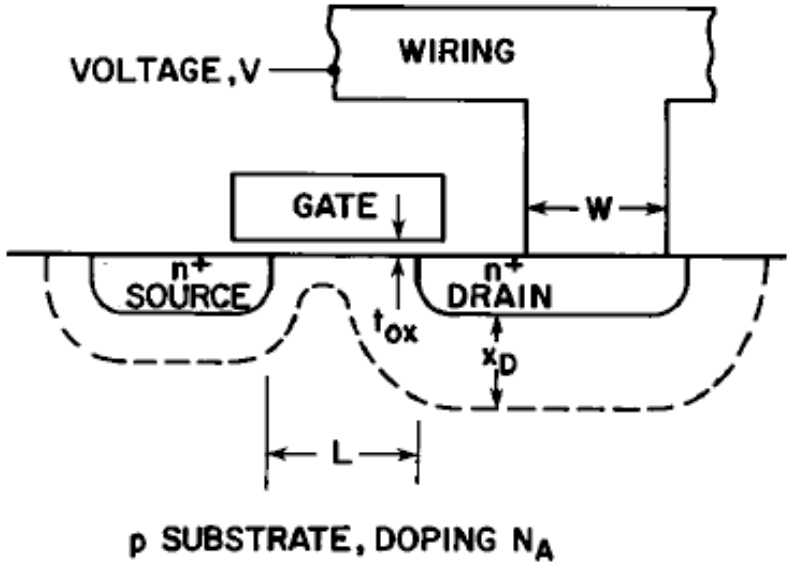
MOSFET Scaling

Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	1/κ
Doping concentration *Na*	κ
Voltage *V*	1/κ
Current *I*	1/κ
Capacitance *εA/t*	1/κ
Delay time/circuit *VC/I*	1/κ
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1



R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling was first described by Dennard in 1974

MOSFET Scaling

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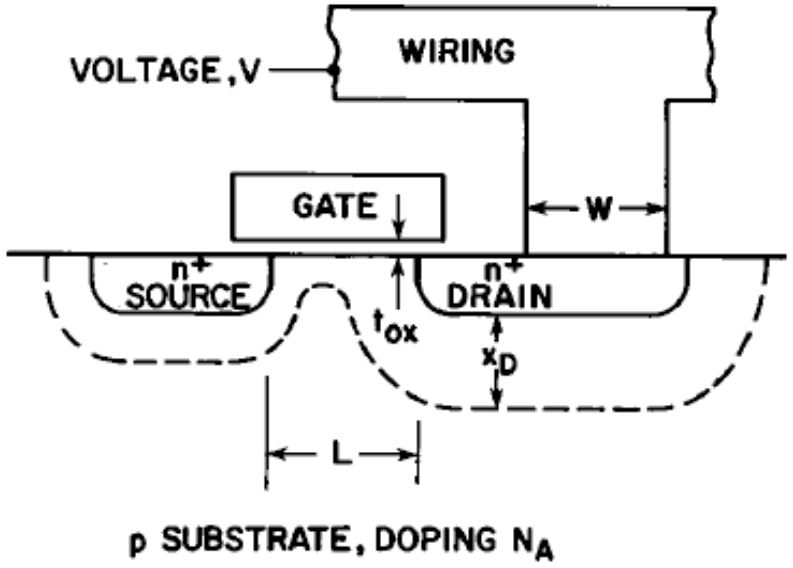
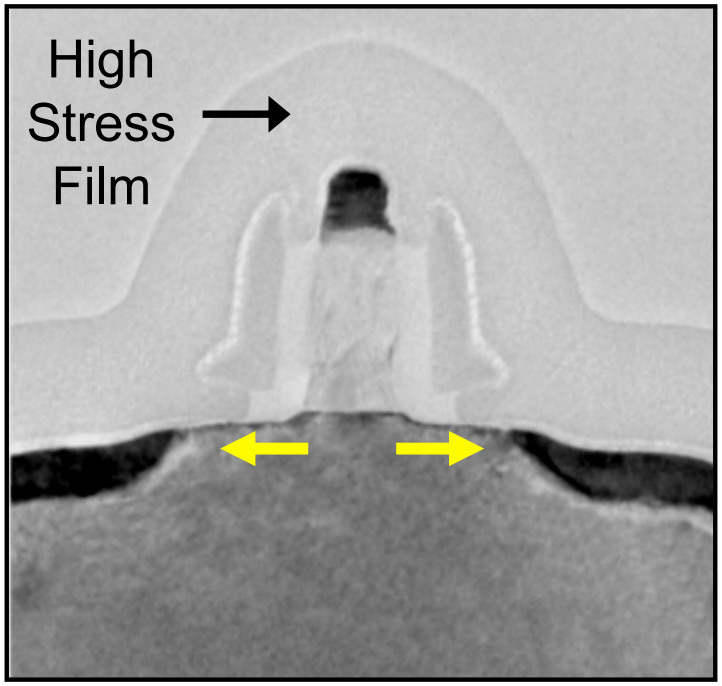


R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling ENDED at the 130nm node (and nobody noticed …)

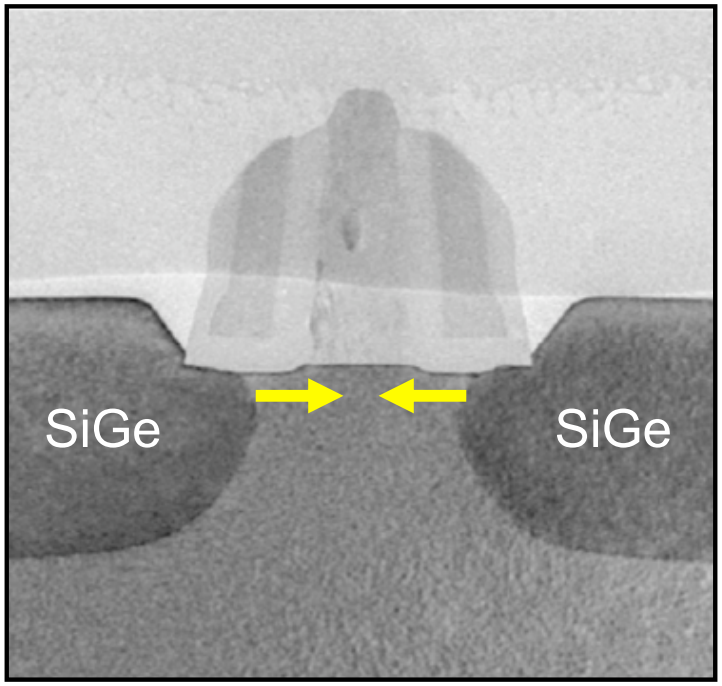
90 nm Strained Silicon Transistors

NMOS



SiN cap layer
Tensile channel strain

PMOS

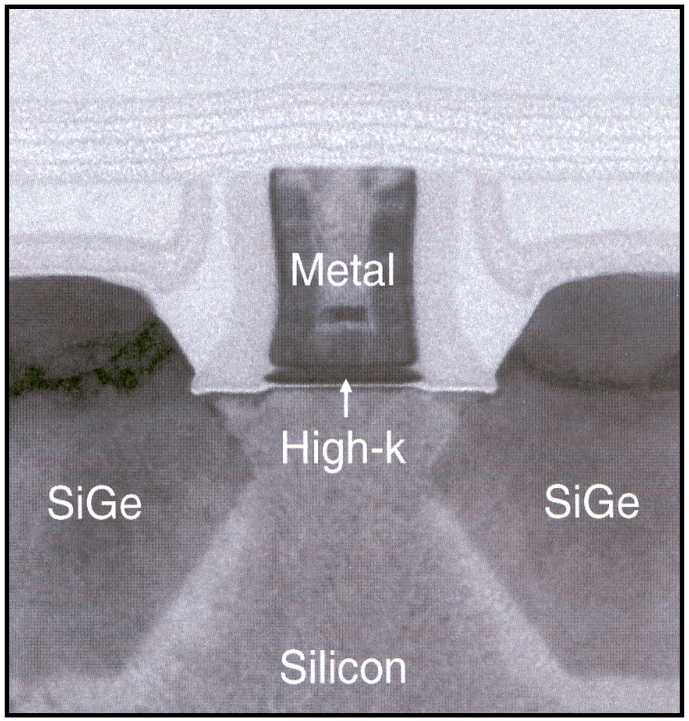


SiGe source-drain
Compressive channel strain

Strained silicon provided increased drive currents, making up for the loss of classical Dennard scaling

45nm High-k + Metal Gate Transistors

45 nm HK+MG



Hafnium-based dielectric

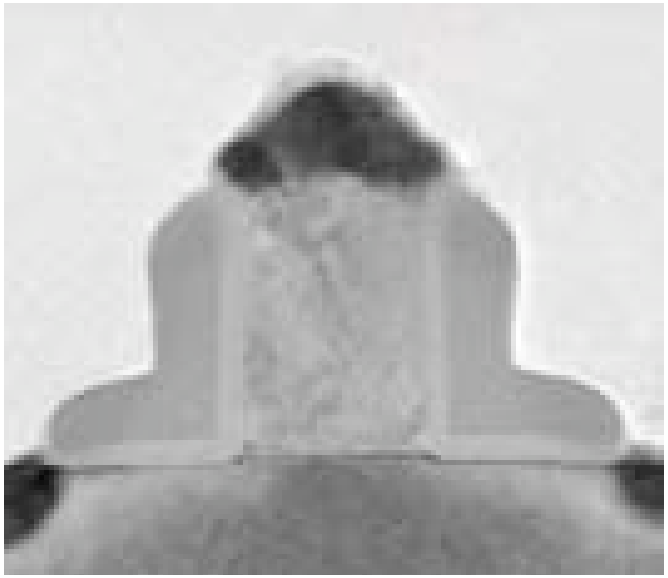
Metal gate electrode

High-k + metal gate transistors restored gate oxide scaling at the 45nm node

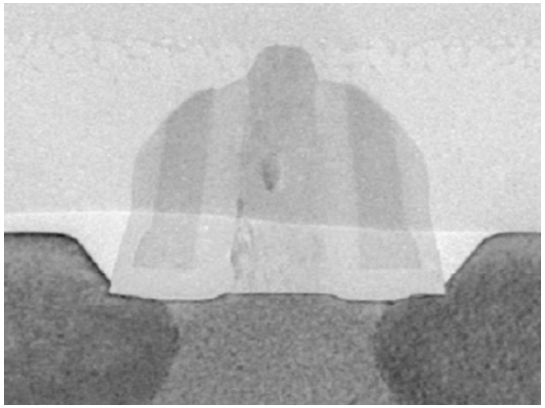
Changes in Scaling

THEN

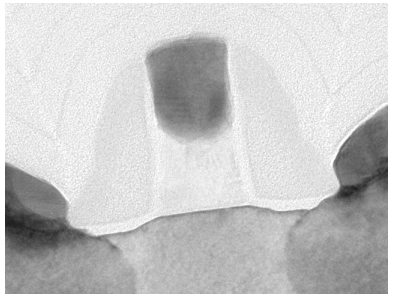
- Scaling drove down cost
- Scaling drove performance
- Performance constrained
- Active power dominates
- Independent design-process



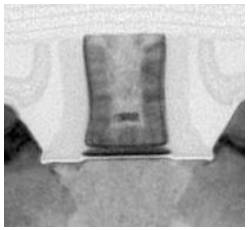
130nm



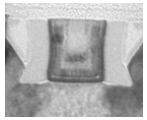
90nm



65nm



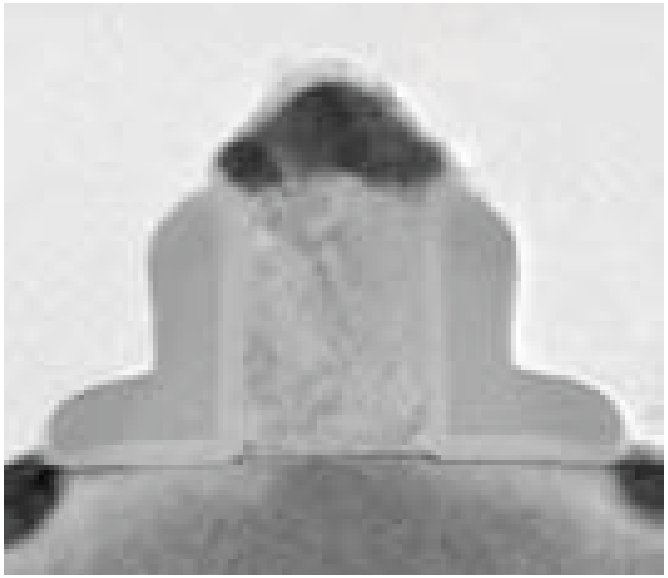
45nm



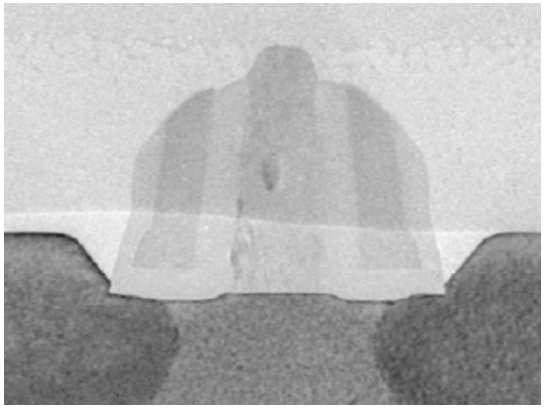
32nm

Changes in Scaling

THEN	NOW
• Scaling drove down cost	• Scaling drives down cost
• Scaling drove performance	• Materials drive performance
• Performance constrained	• Power constrained
• Active power dominates	• Standby power dominates
• Independent design-process	• Collaborative design-process



130nm



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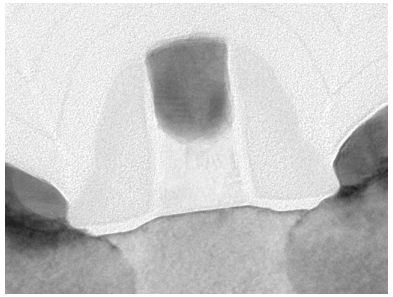

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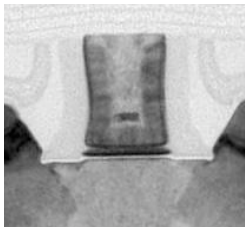

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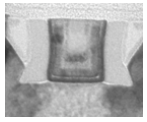
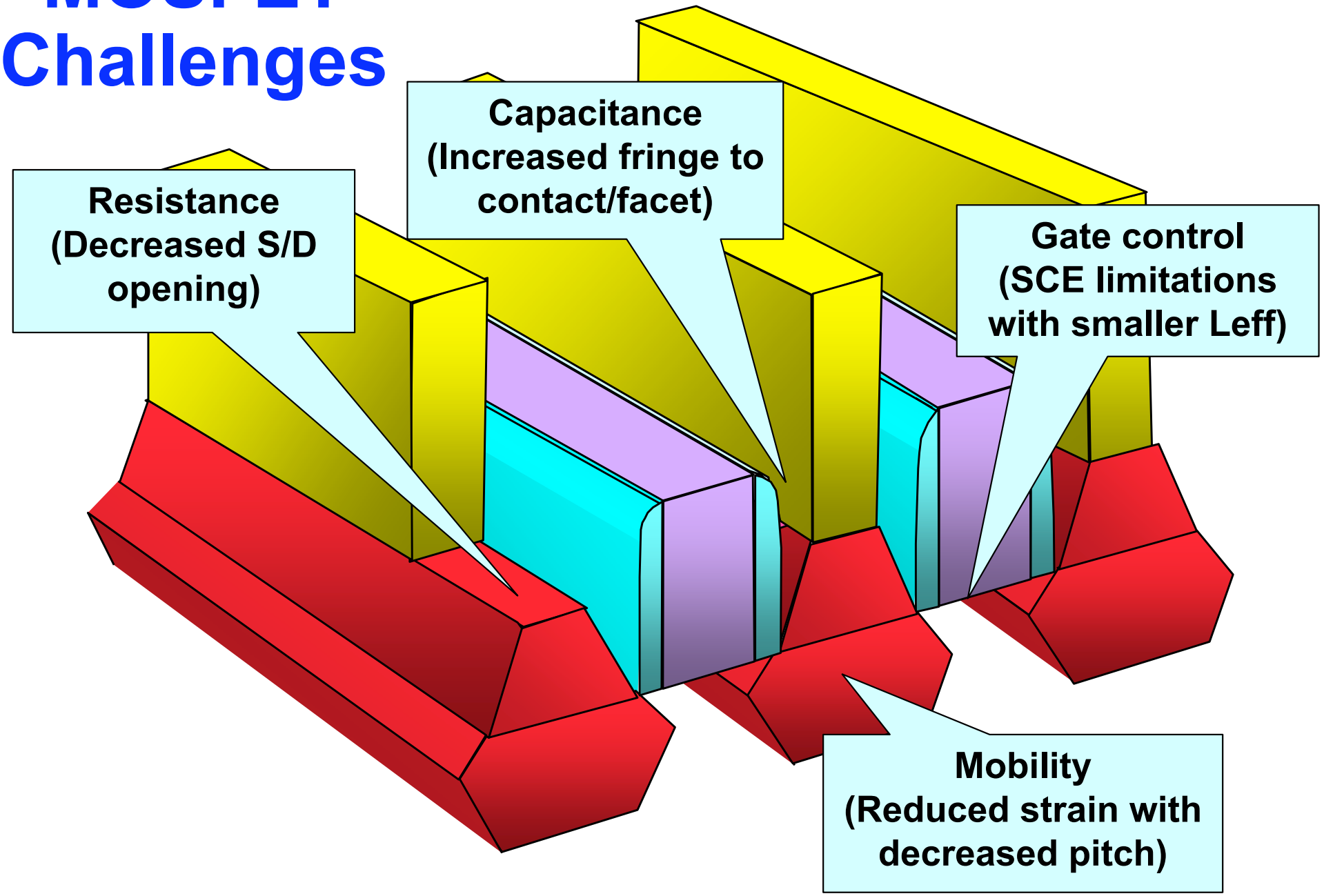


32nm

MOSFET Challenges



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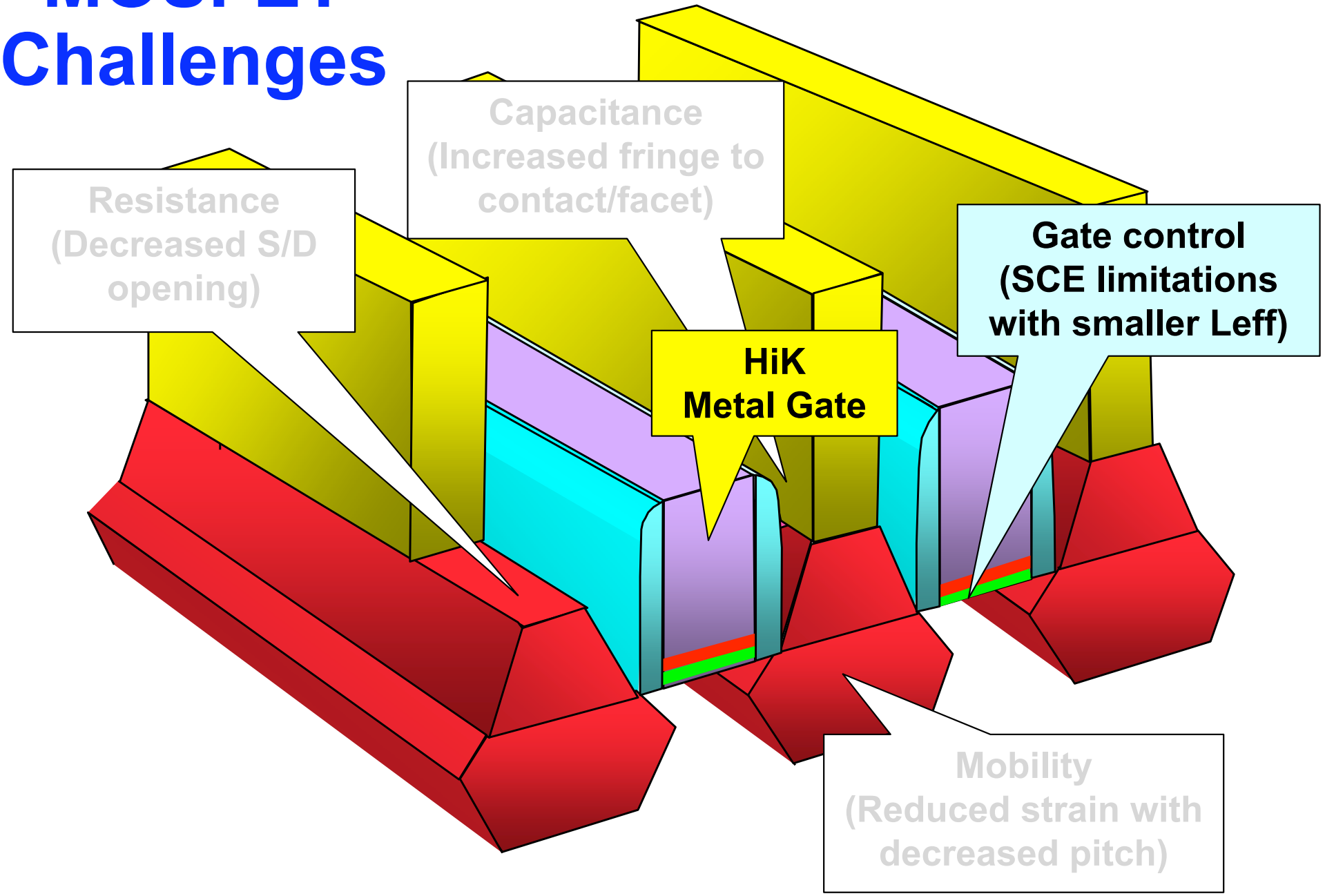


High-k Metal Gate

BENEFITS

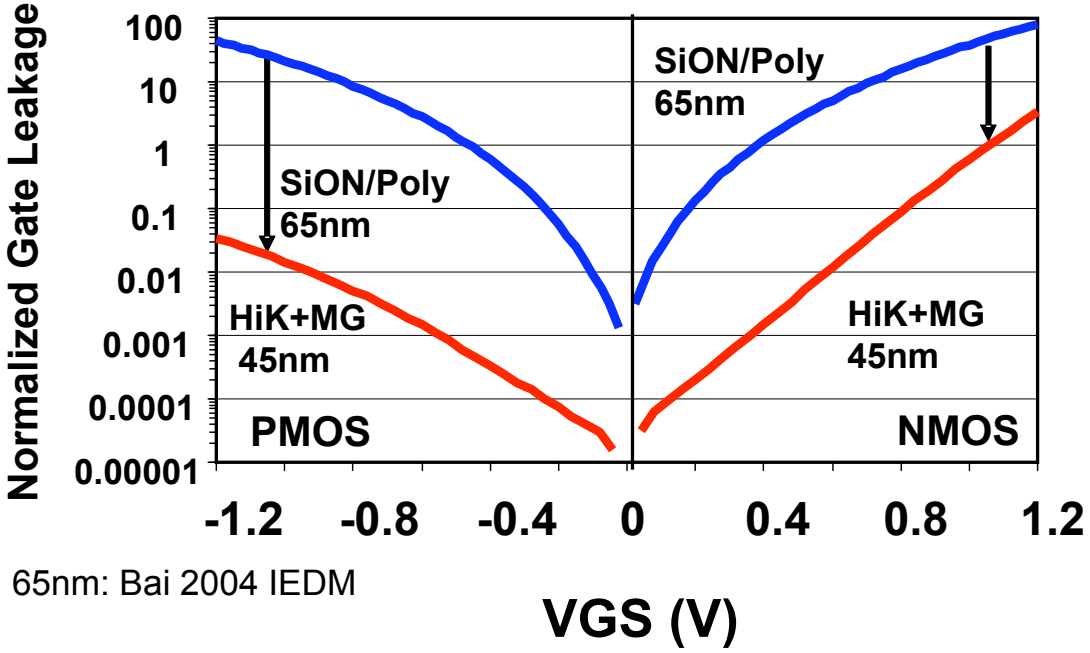
- **High-k gate dielectric**
  - Reduced gate leakage
  - Continued T_{OX} scaling
- **Metal gates**
  - Eliminate polysilicon depletion
  - Resolve V_T pinning for poly on high-k gate dielectrics

CHALLENGES

- **High-k gate dielectric**
  - Reduced reliability
  - Reduced mobility
- **Metal gates**
  - Dual bandedge workfunctions
  - Thermal stability
  - Process integration

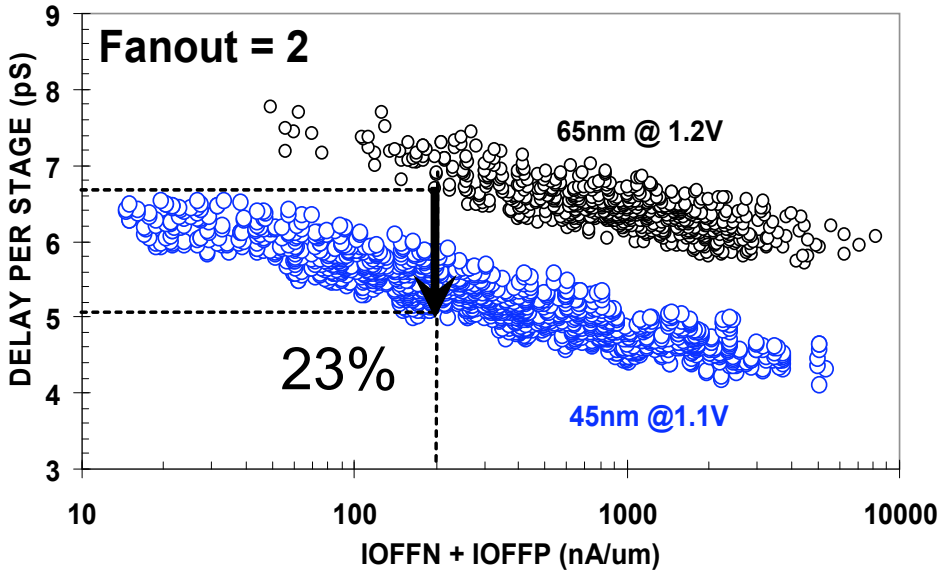
K. Mistry - IEDM 2007

High-k Metal Gate: ToxE and Ig



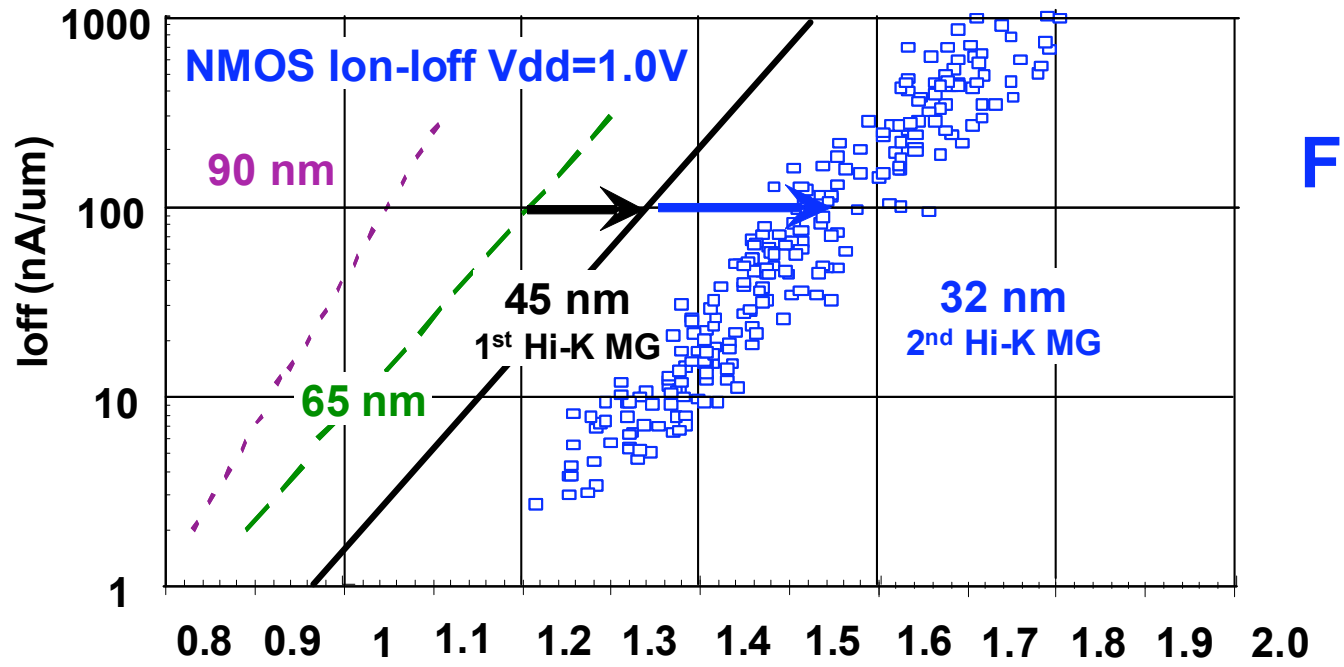
65nm: Bai 2004 IEDM

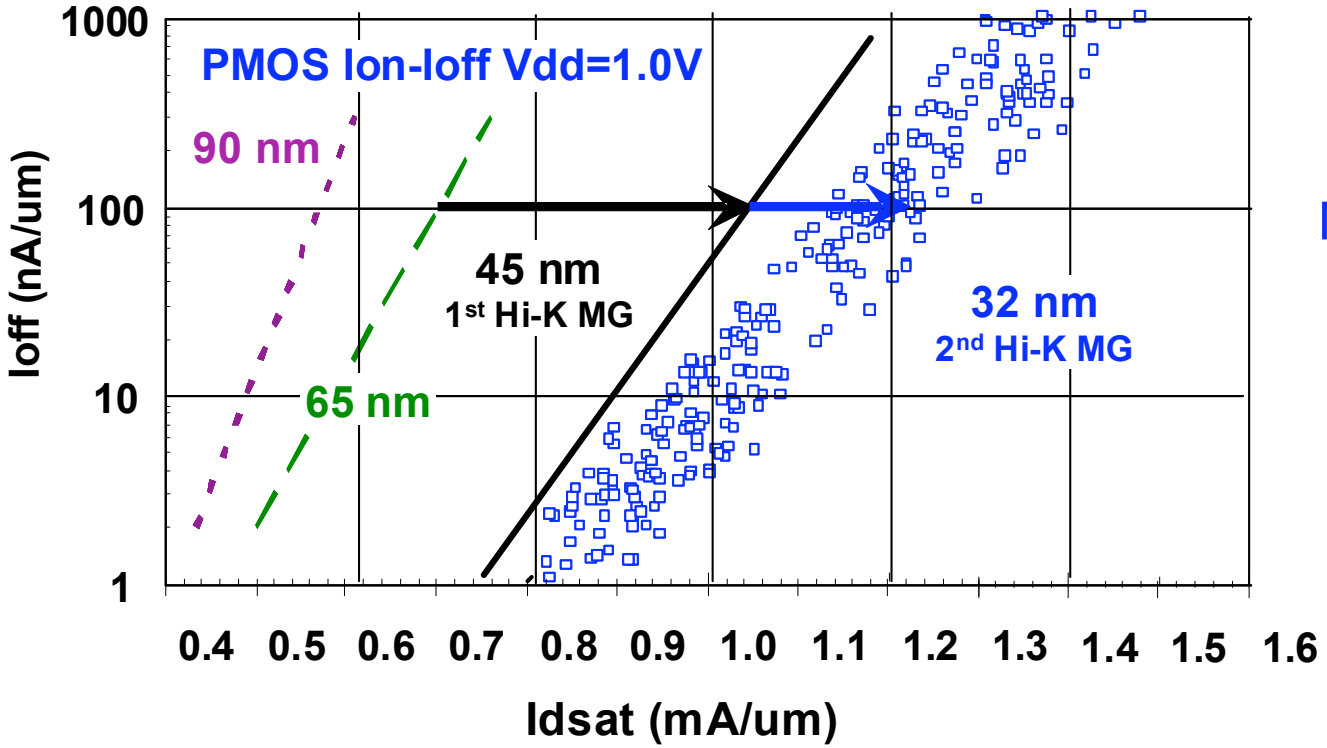
High-k/MG enables 0.7X ToxE scaling while reducing Ig >> 25X for NMOS and 1000X for PMOS



23% better than 65 nm at the same leakage and 100mV lower Vcc. (FO=2 delay of 5.1 ps at $I_{OFFN} = I_{OFFP} = 100$ nA/μm)

K. Mistry - IEDM 2007



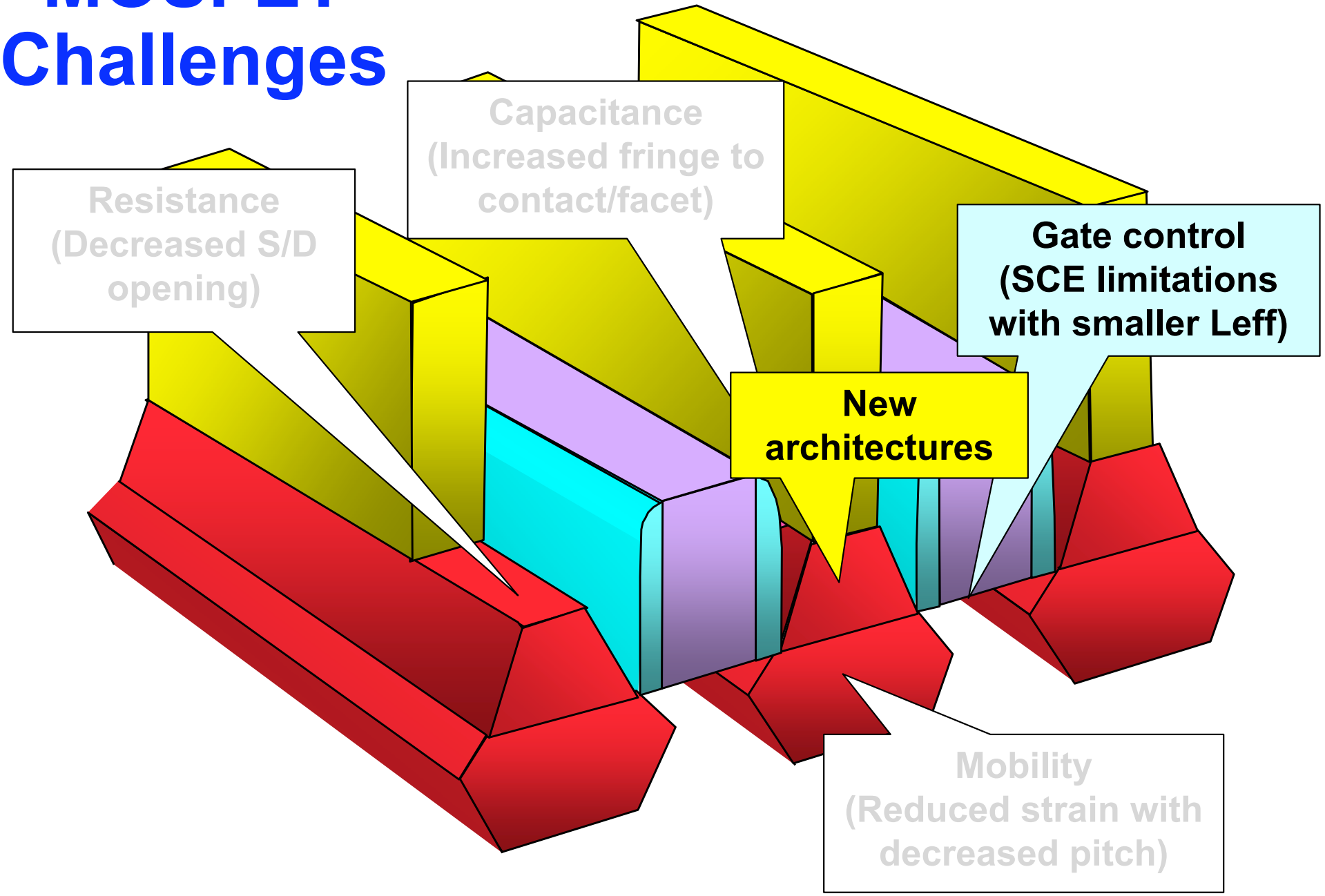


FOUR GENERATION COMPARISON

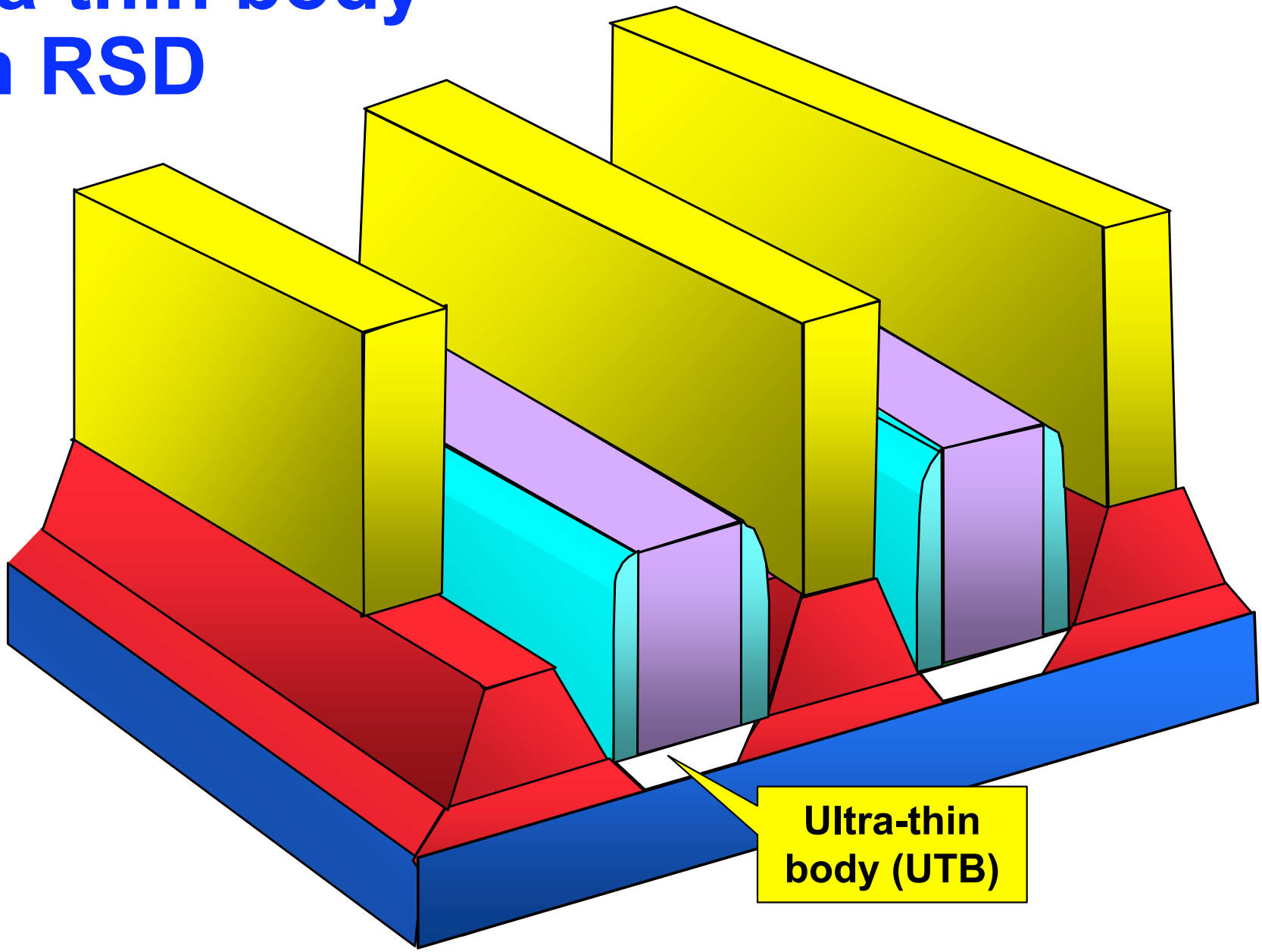
45nm:
1st gen. HiK-MG
Mistry, Intel, IEDM 2007

32nm:
2nd gen. HiK-MG
Natarajan, Intel, IEDM 2008

MOSFET Challenges



Ultra-thin body with RSD



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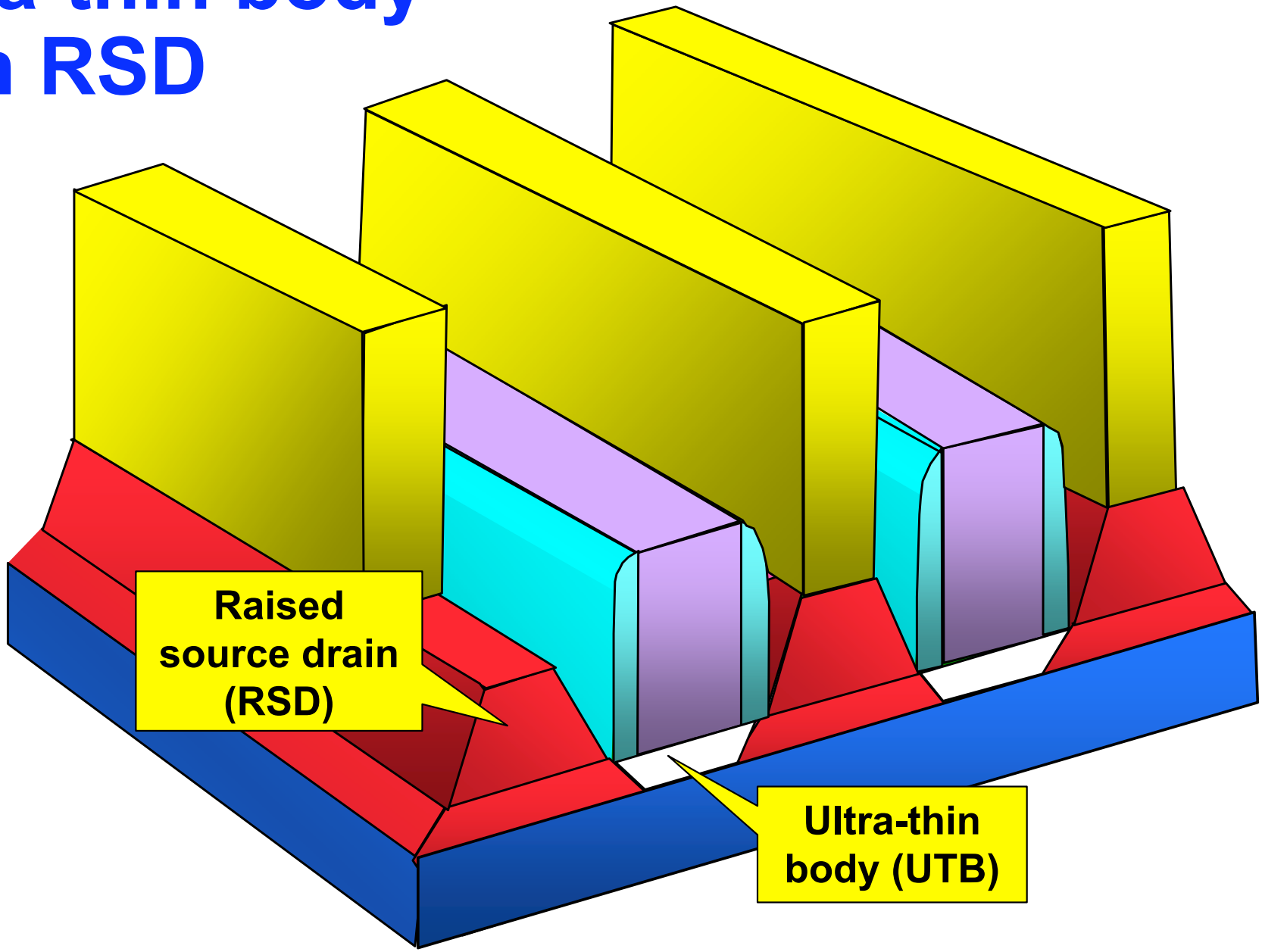
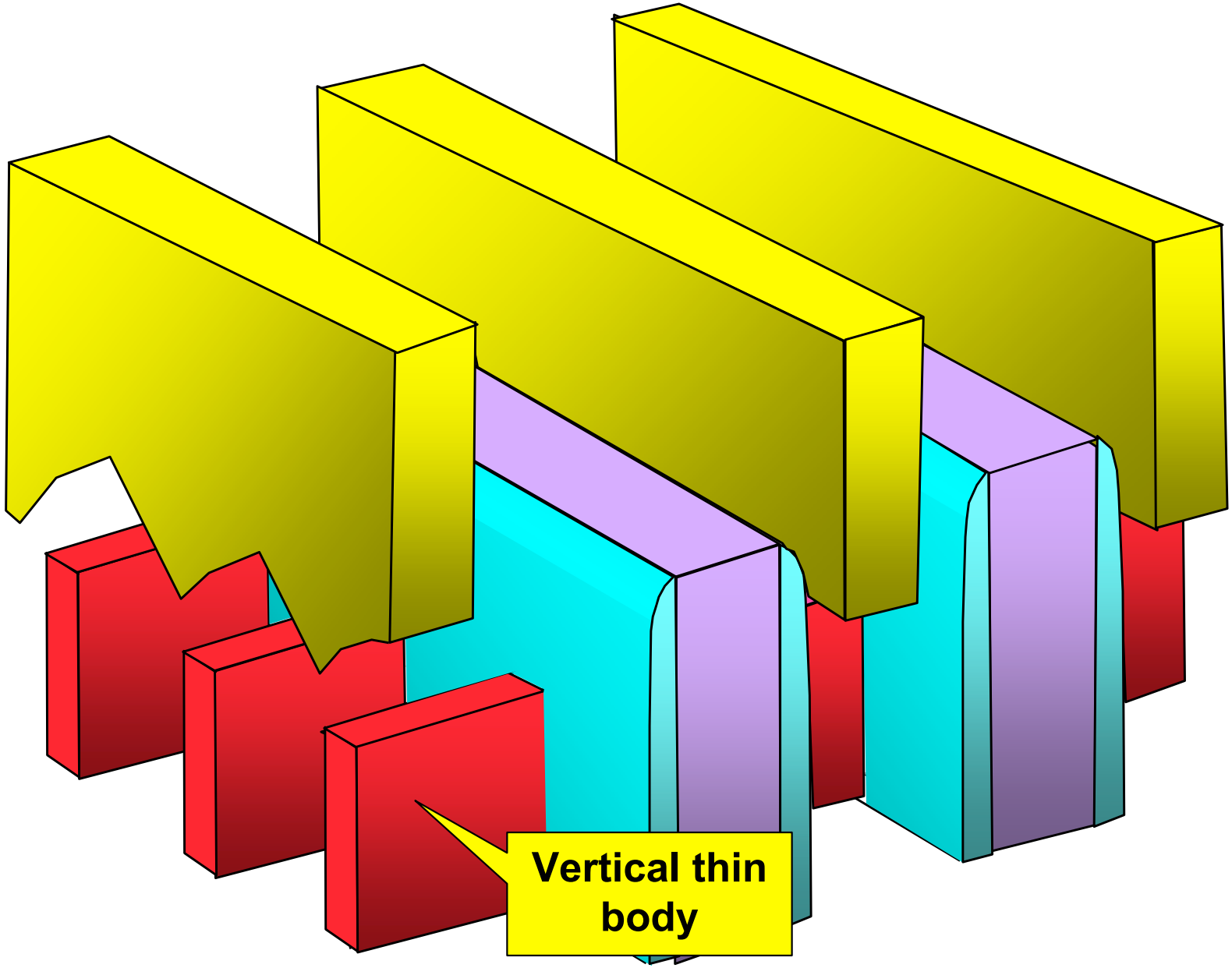


MuGFET



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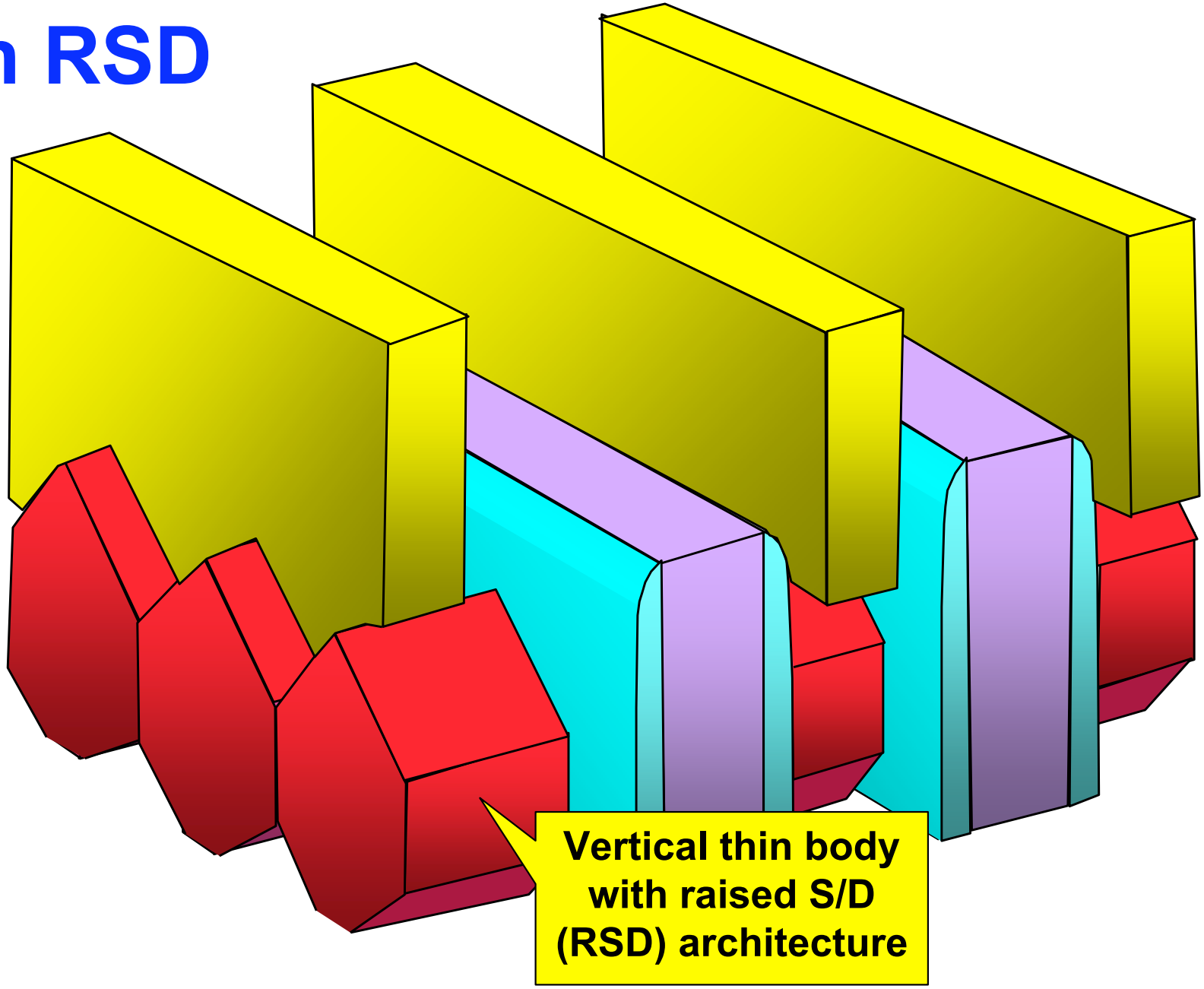
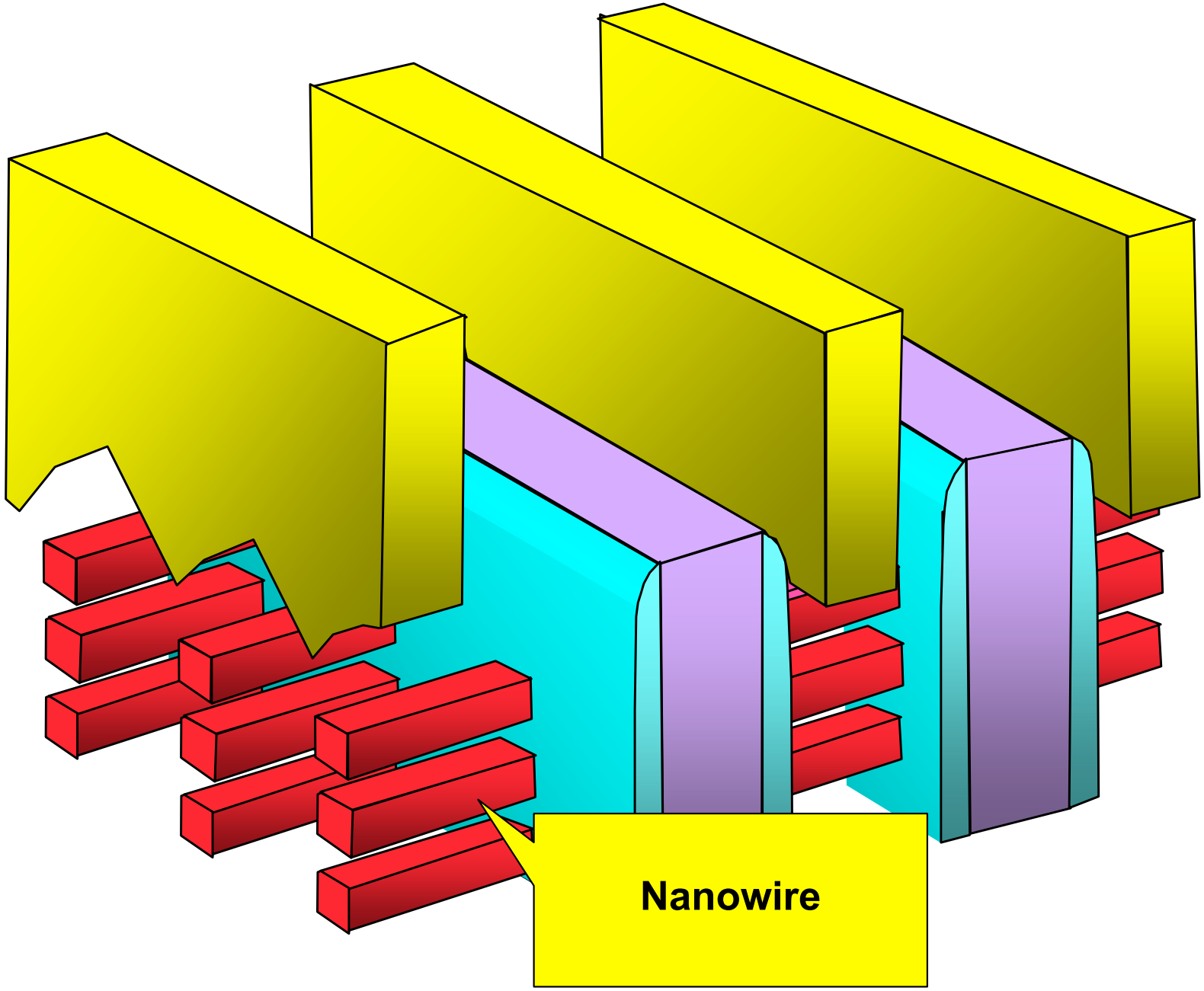
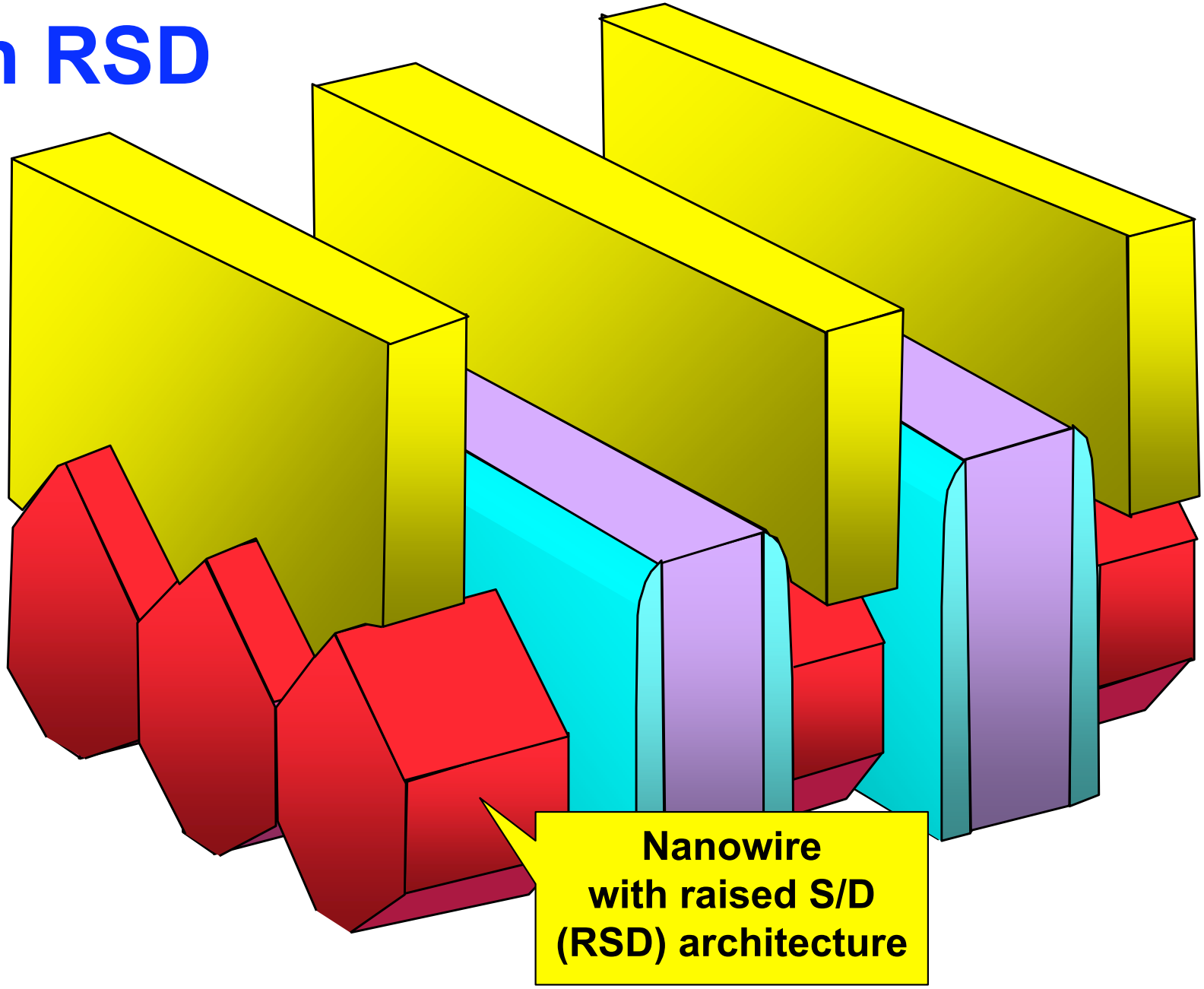


Nanowire



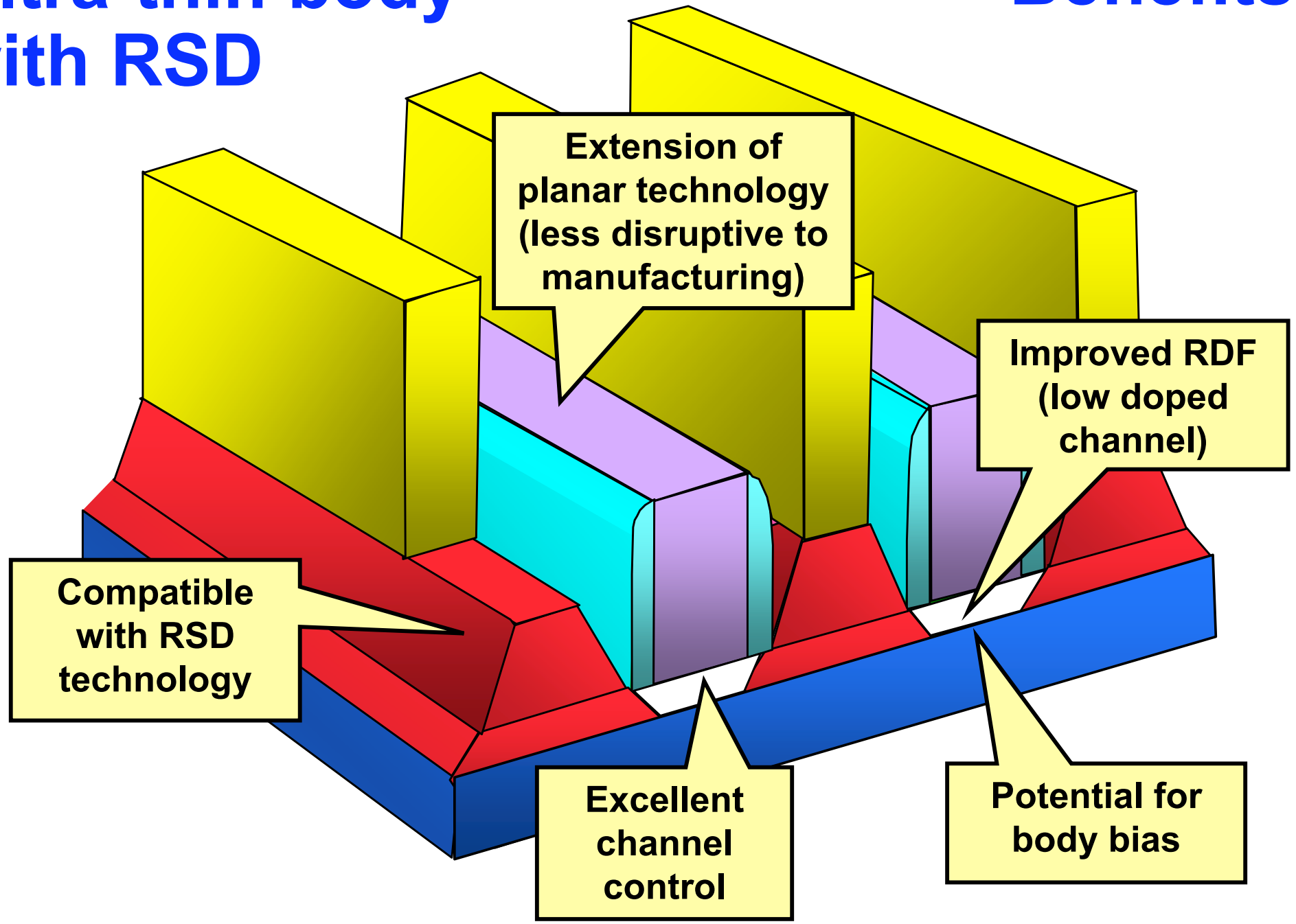
Nanowire with RSD



Looking at all these in more detail

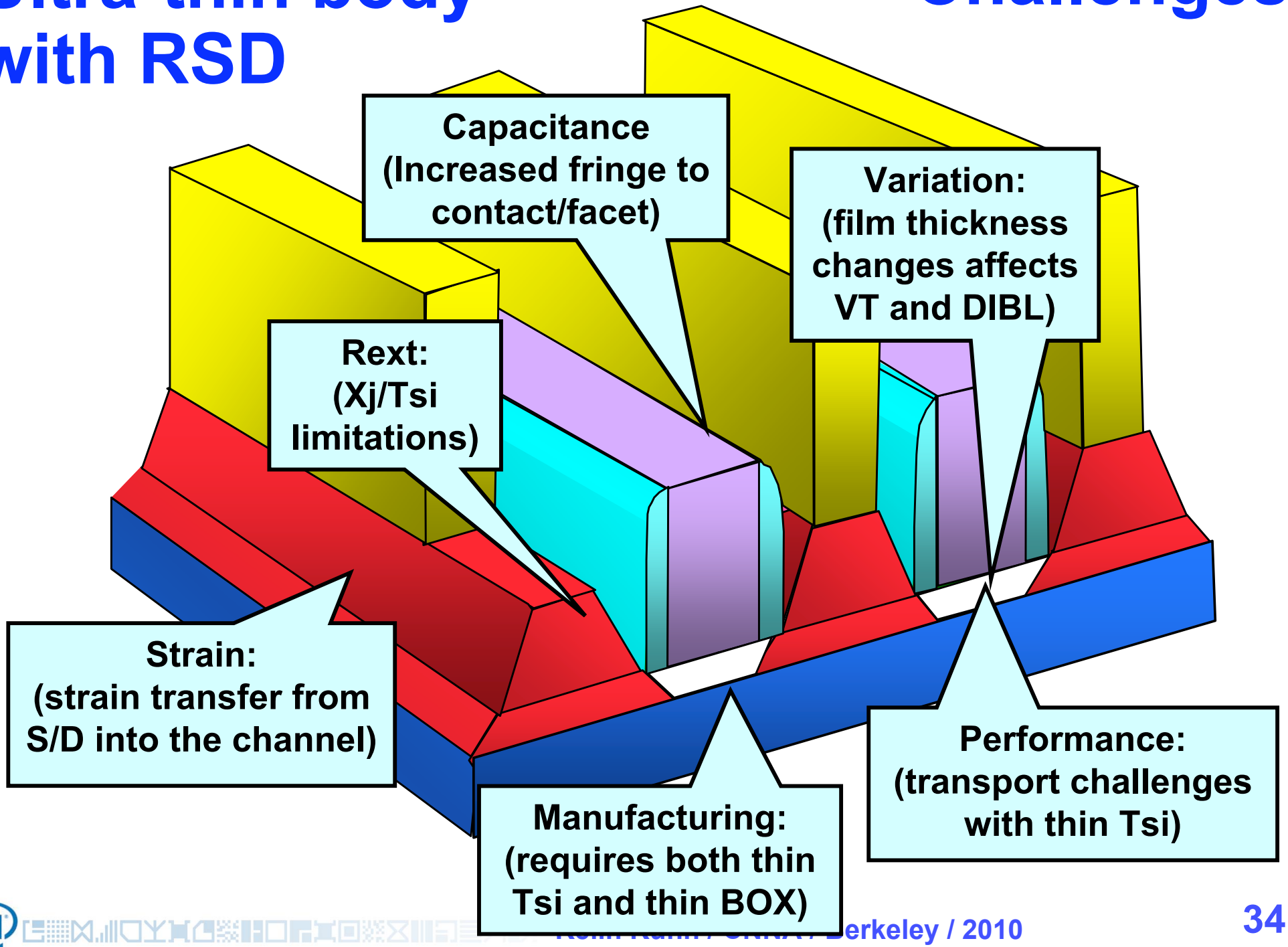
Ultra-thin body with RSD

Benefits



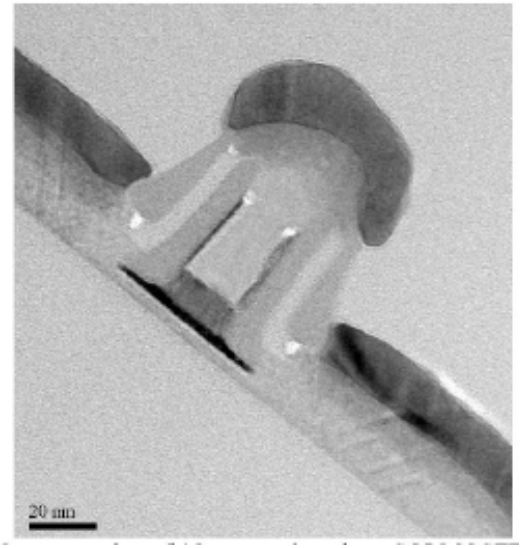
Ultra-thin body with RSD

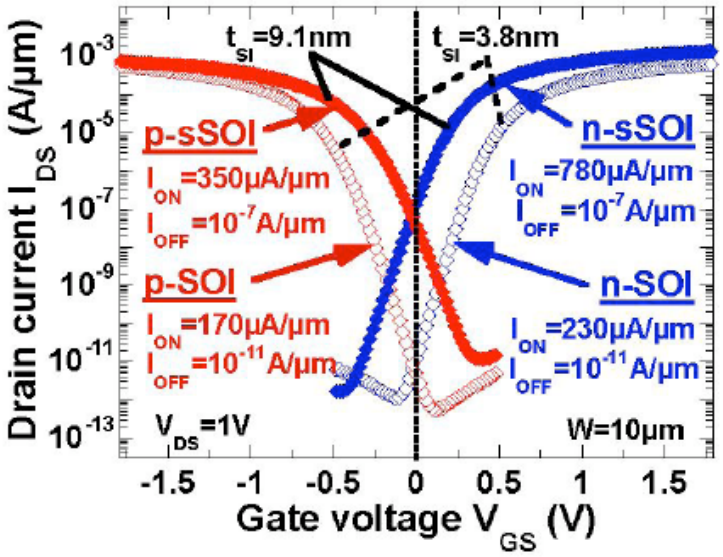
Challenges

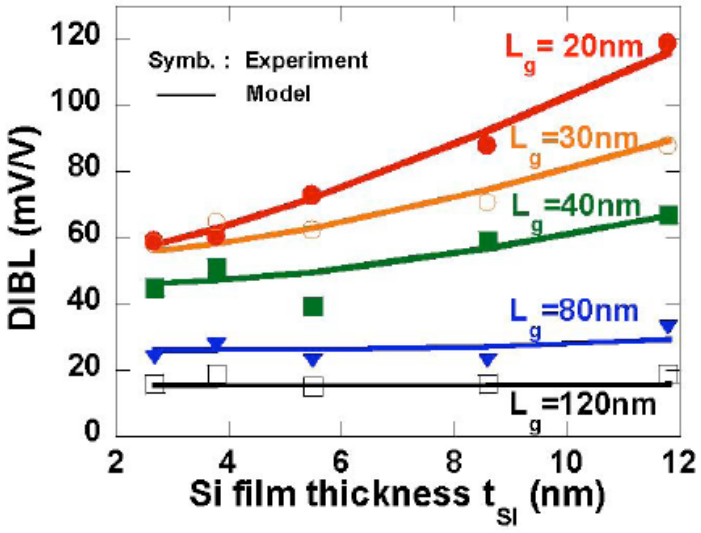


Ultra-thin body

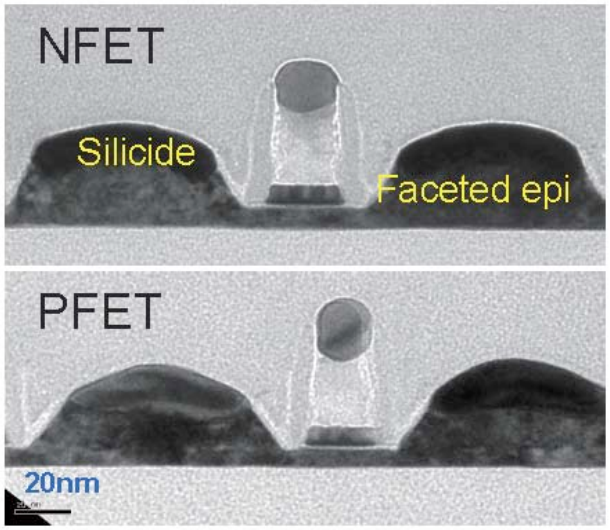
Barral – CEA-LETI– IEDM 2007

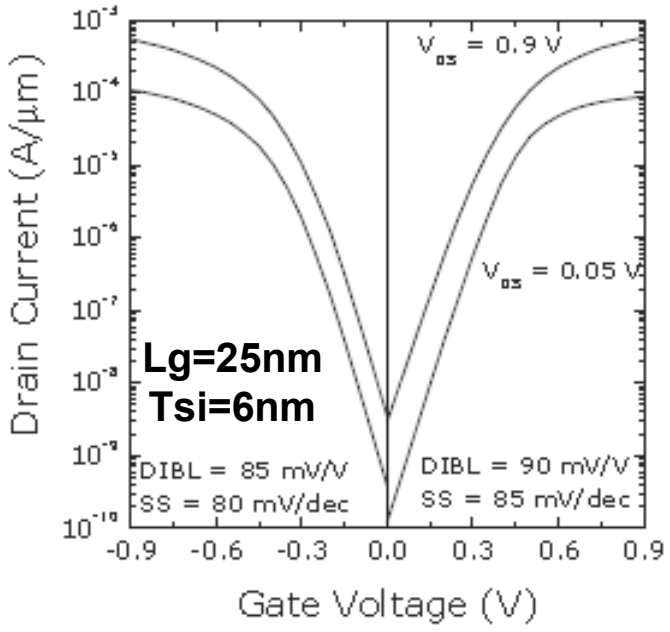


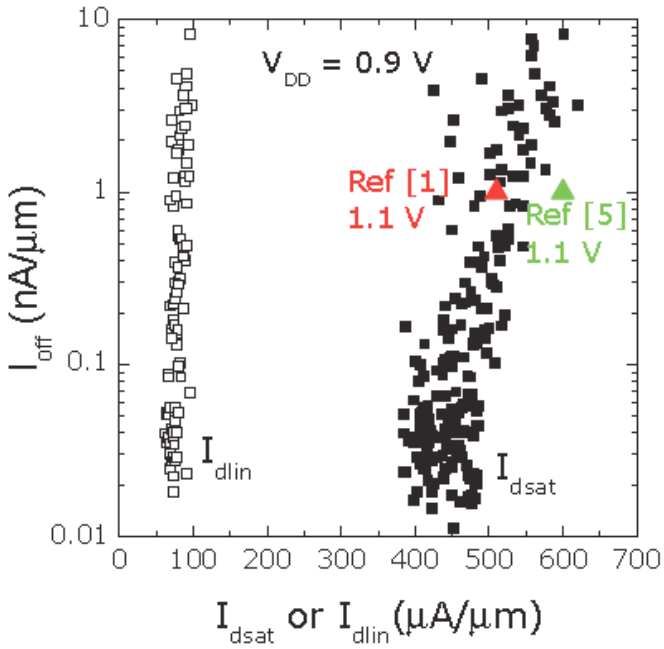




Cheng – IBM – VLSI 2009

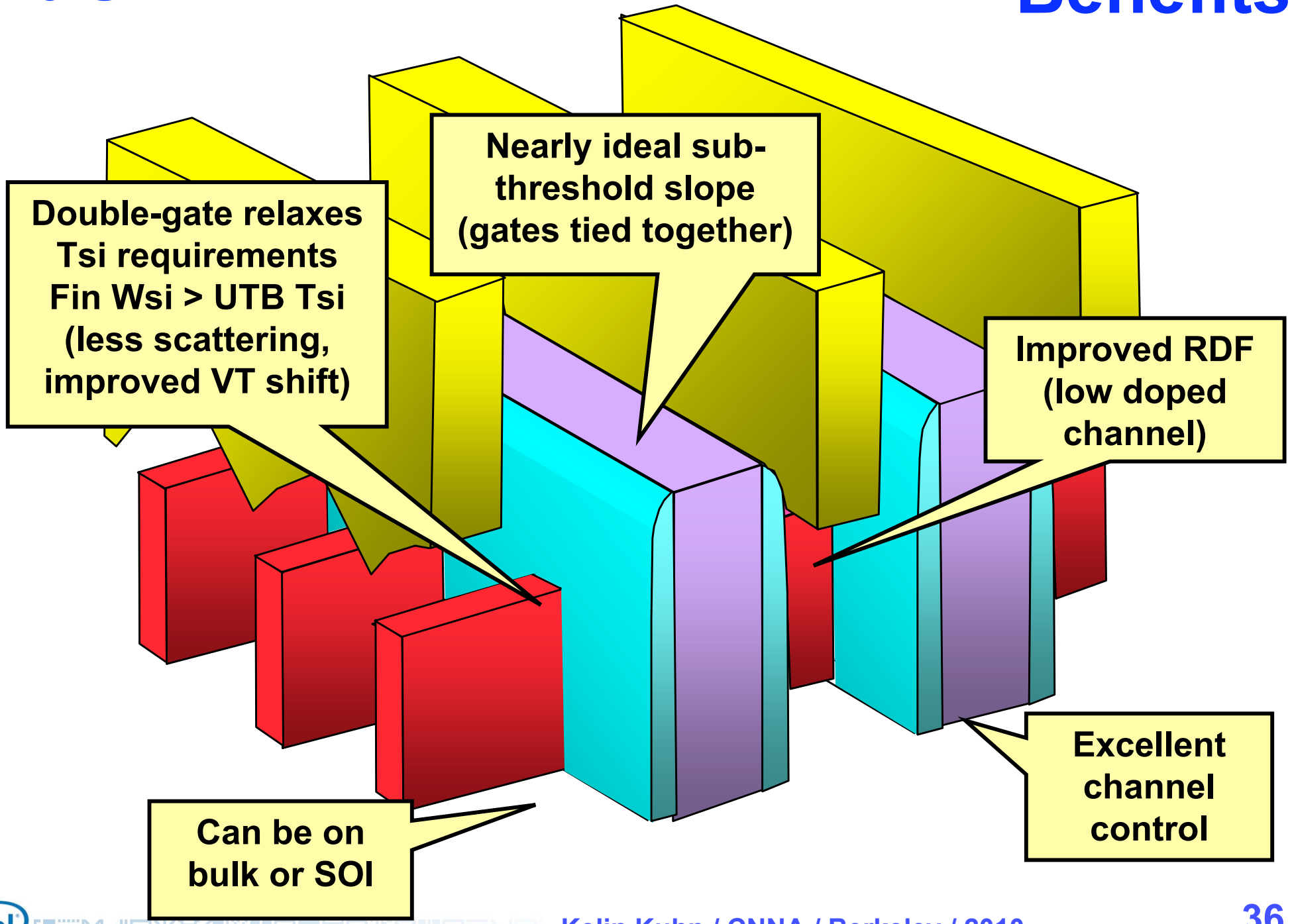






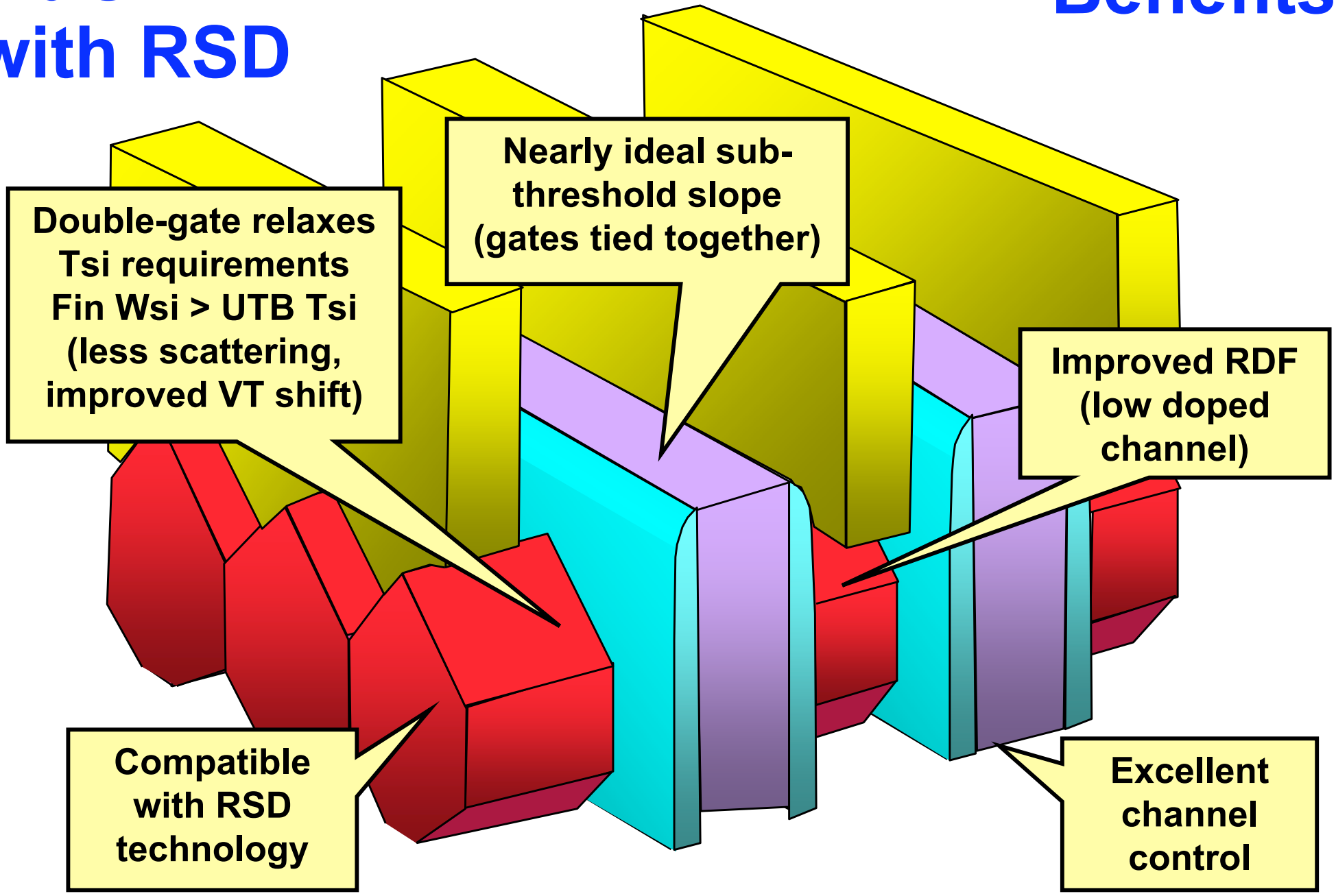
MuGFET

Benefits



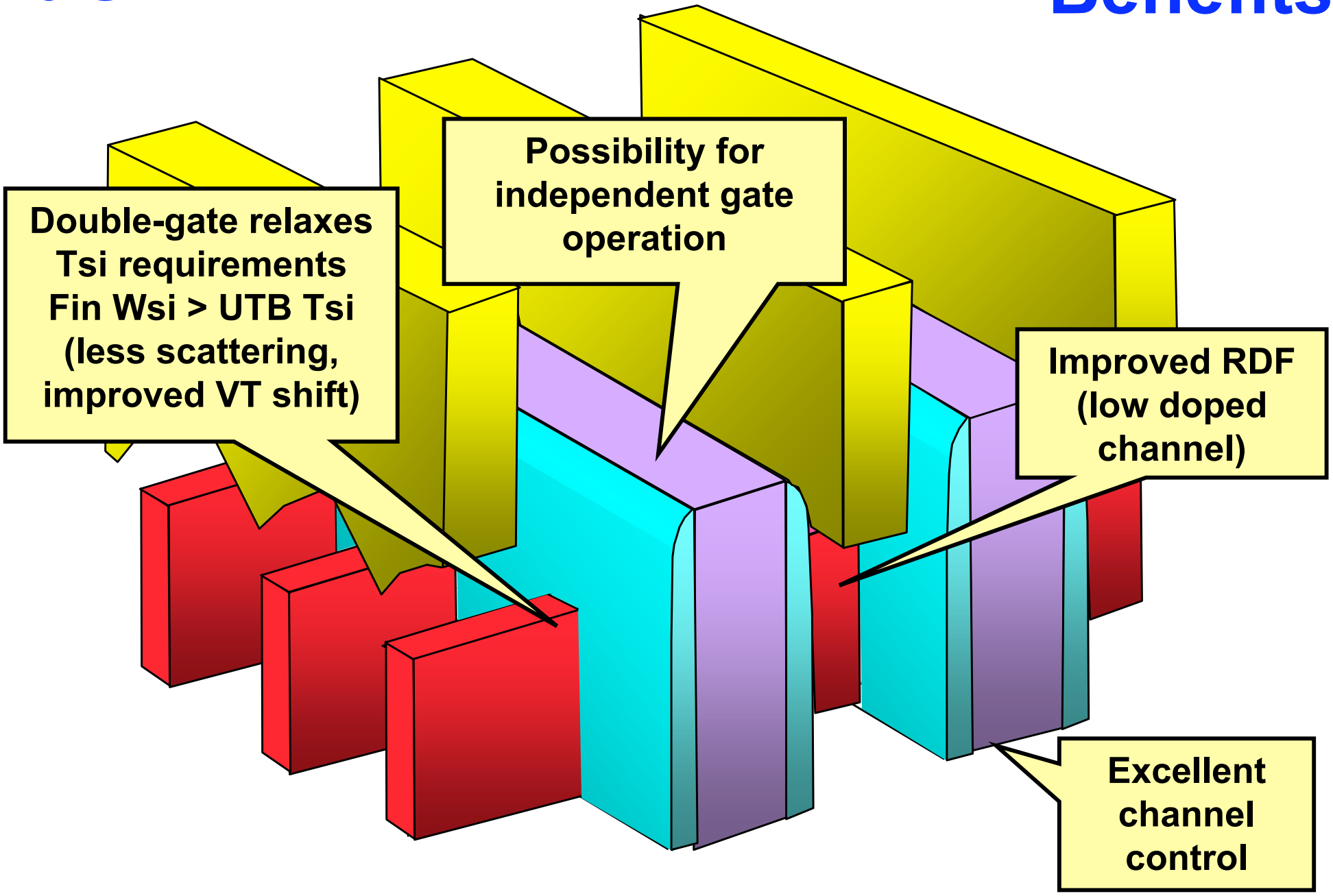
MuGFET with RSD

Benefits



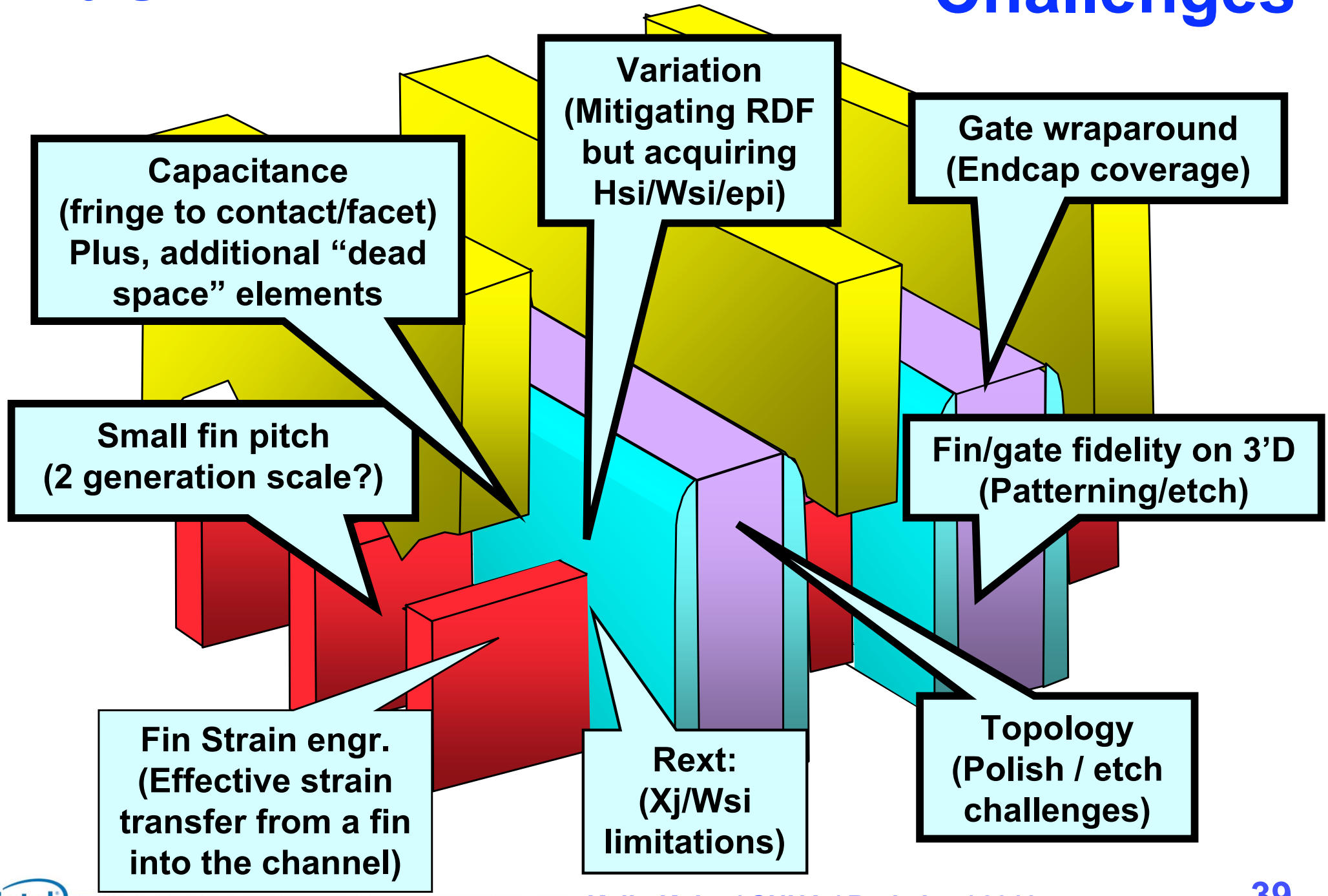
MuGFET

Benefits



MuGFET

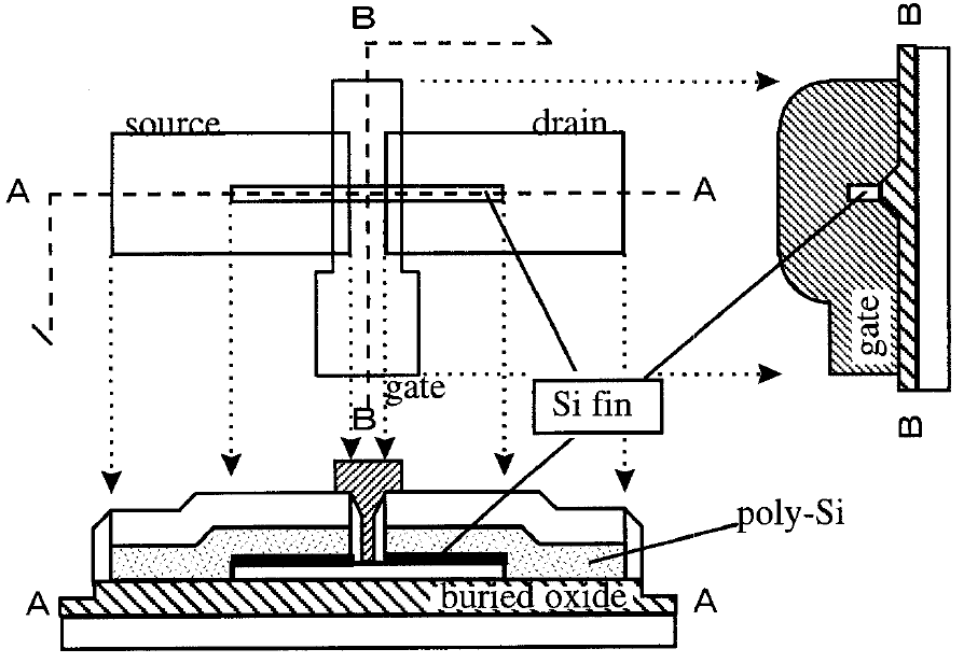
Challenges



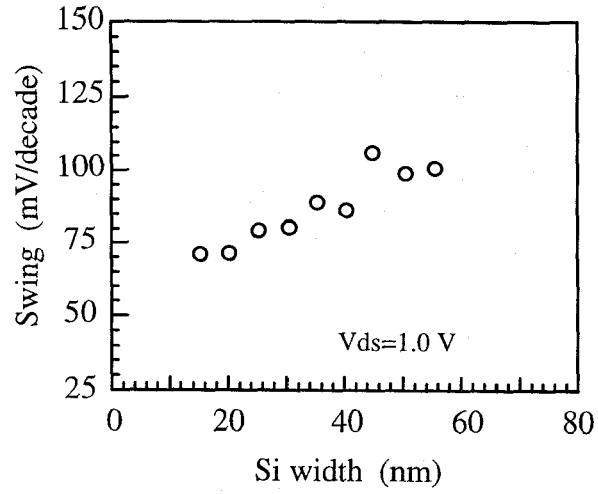
Hisamoto – Hitachi / Berkeley– IEDM 1998 [3]

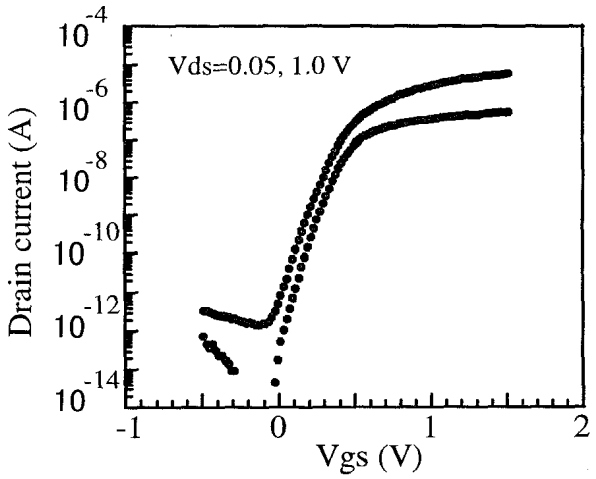
A Folded-channel MOSFET for Deep-sub-tenth Micron Era

Digh Hisamoto, Wen-Chin Lee*, Jakub Kedzierski*, Erik Anderson**, Hideki Takeuchi+,
Kazuya Asano++, Tsu-Jae King*, Jeffrey Bokor*, and Chenming Hu*
Central Research Laboratory, Hitachi Ltd., *) EECS, UC Berkeley,
**) Lawrence Berkeley Laboratory, +) Nippon Steel Corp., ++) NKK Corp.



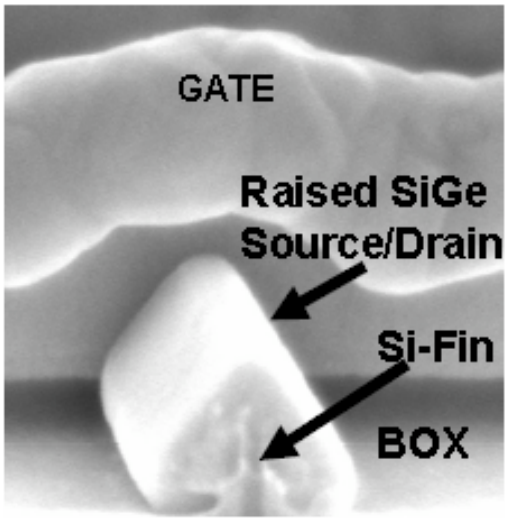
. 1 Folded channel MOSFET layout design and device structure.
: bottom is A-A cross section, and the right is B-B cross section

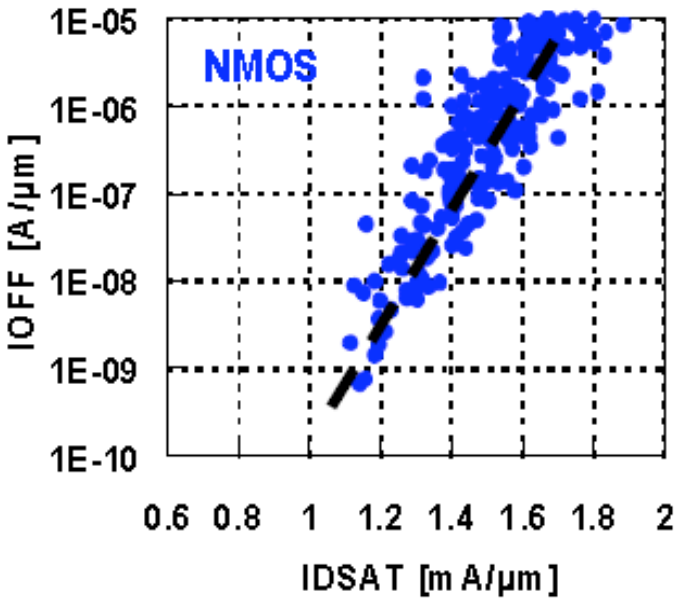


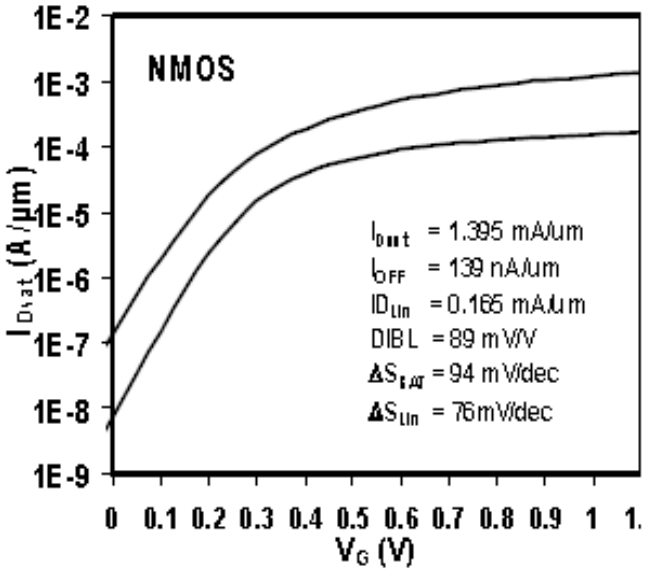


MuGFET

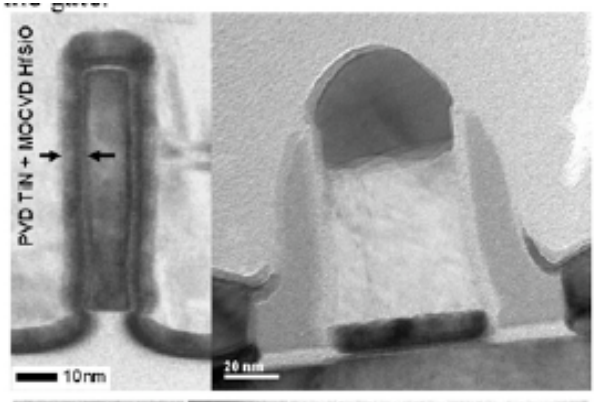
Kavalieros – Intel – IEDM 2006

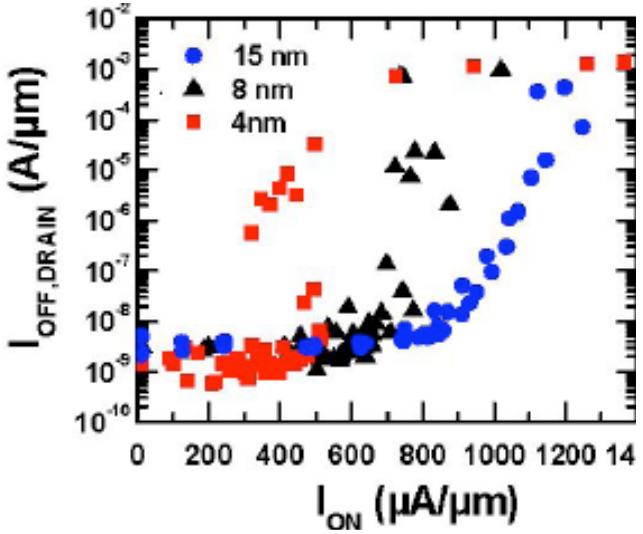


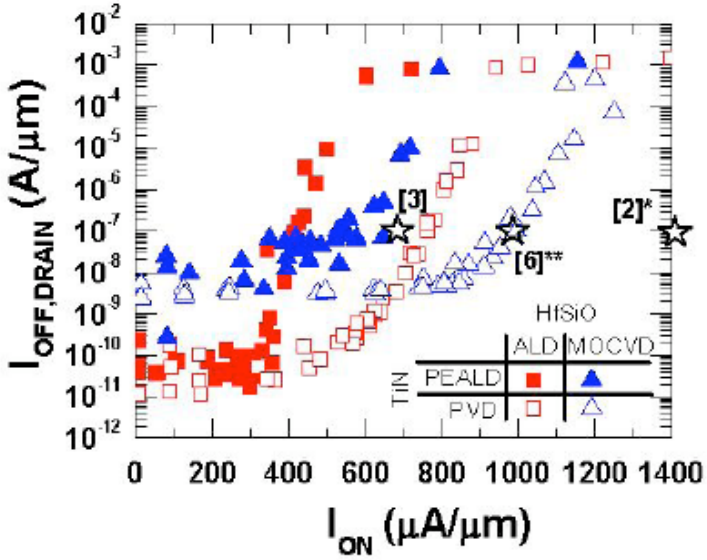




Vellianitis – NXP-TSMC – IEDM 2007

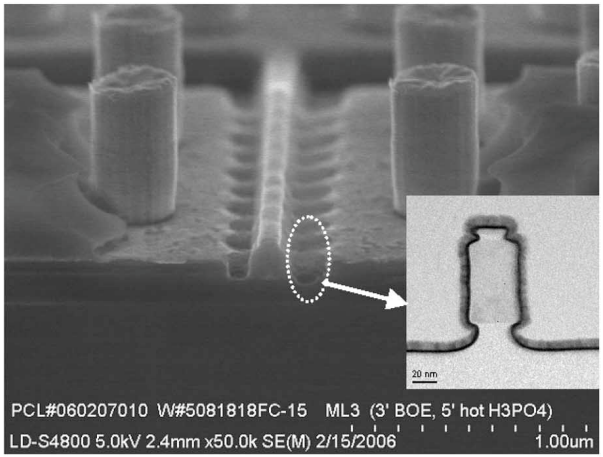


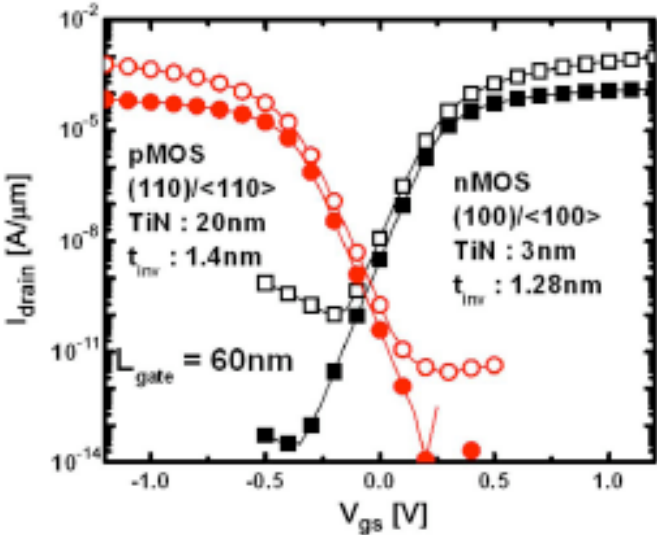


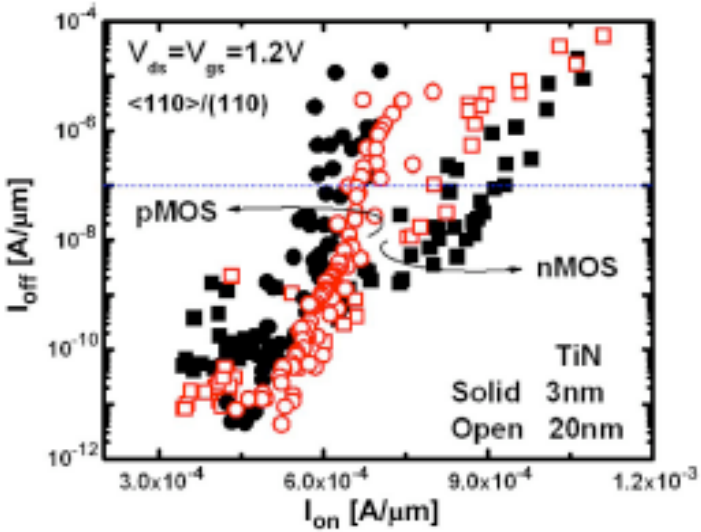


MuGFET

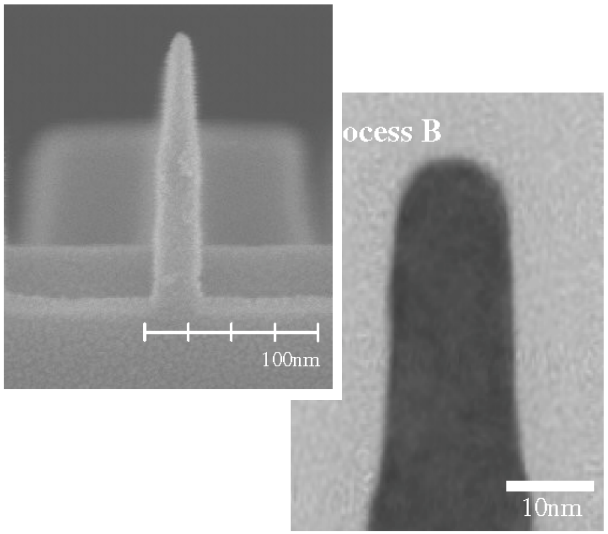
Kang – Sematech – VLSI 2008

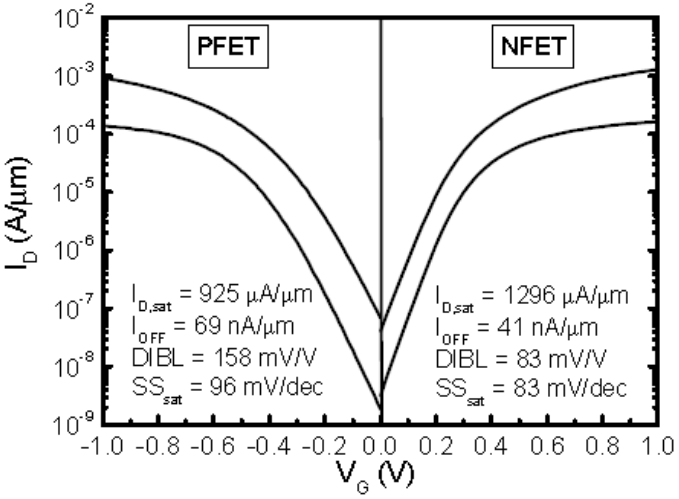


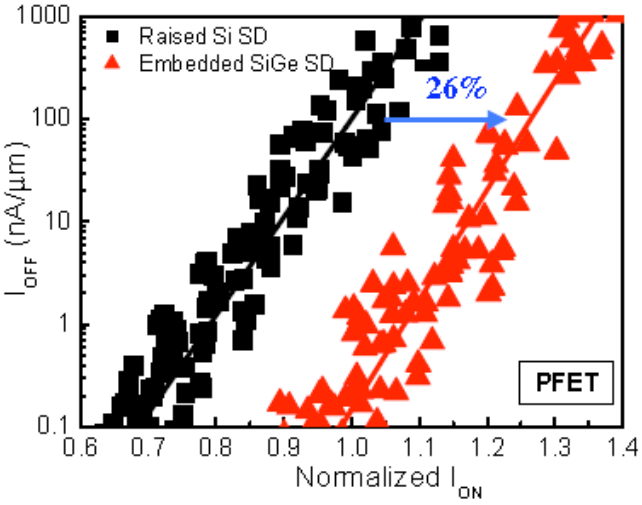




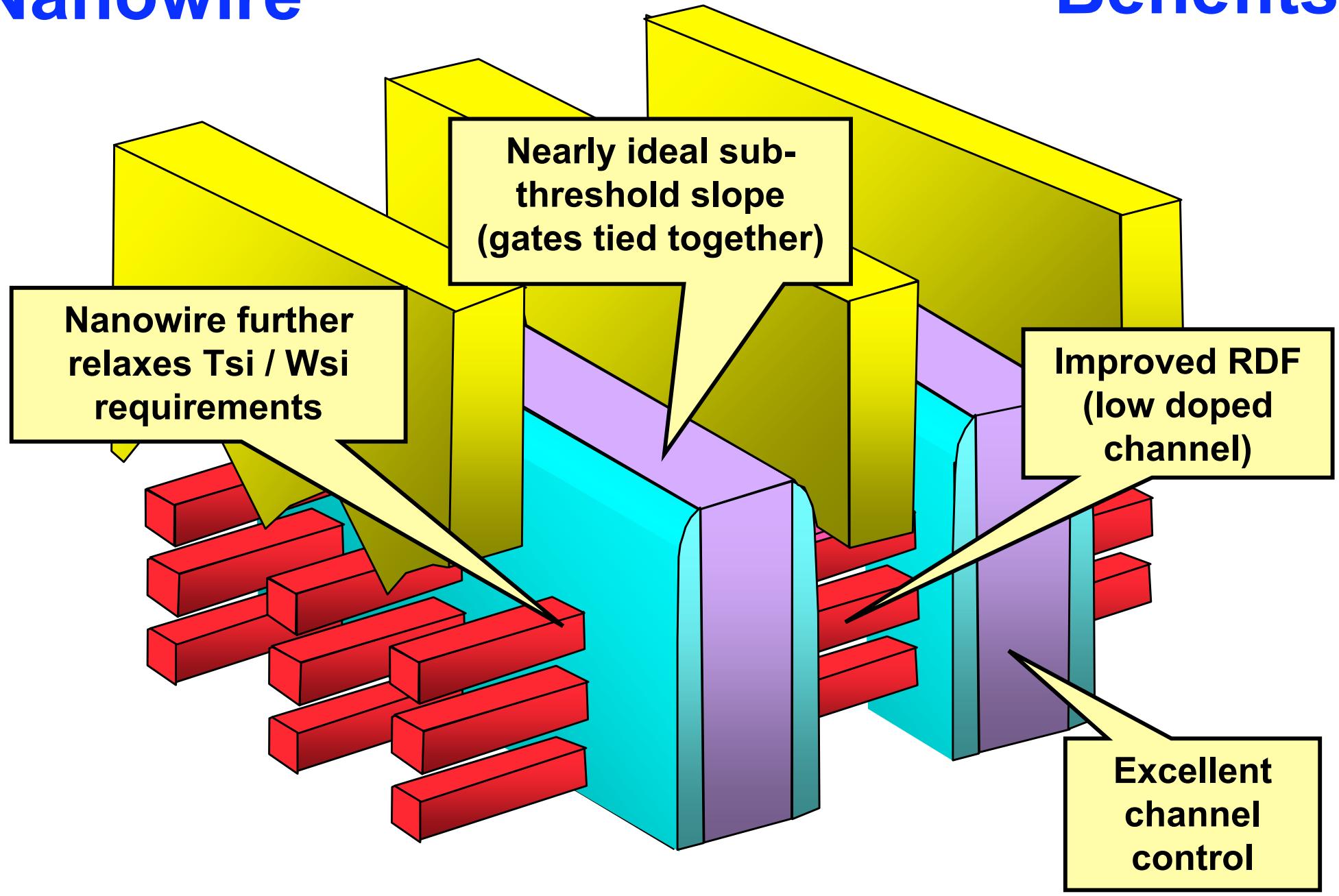
Chang – TSMC – IEDM 2009



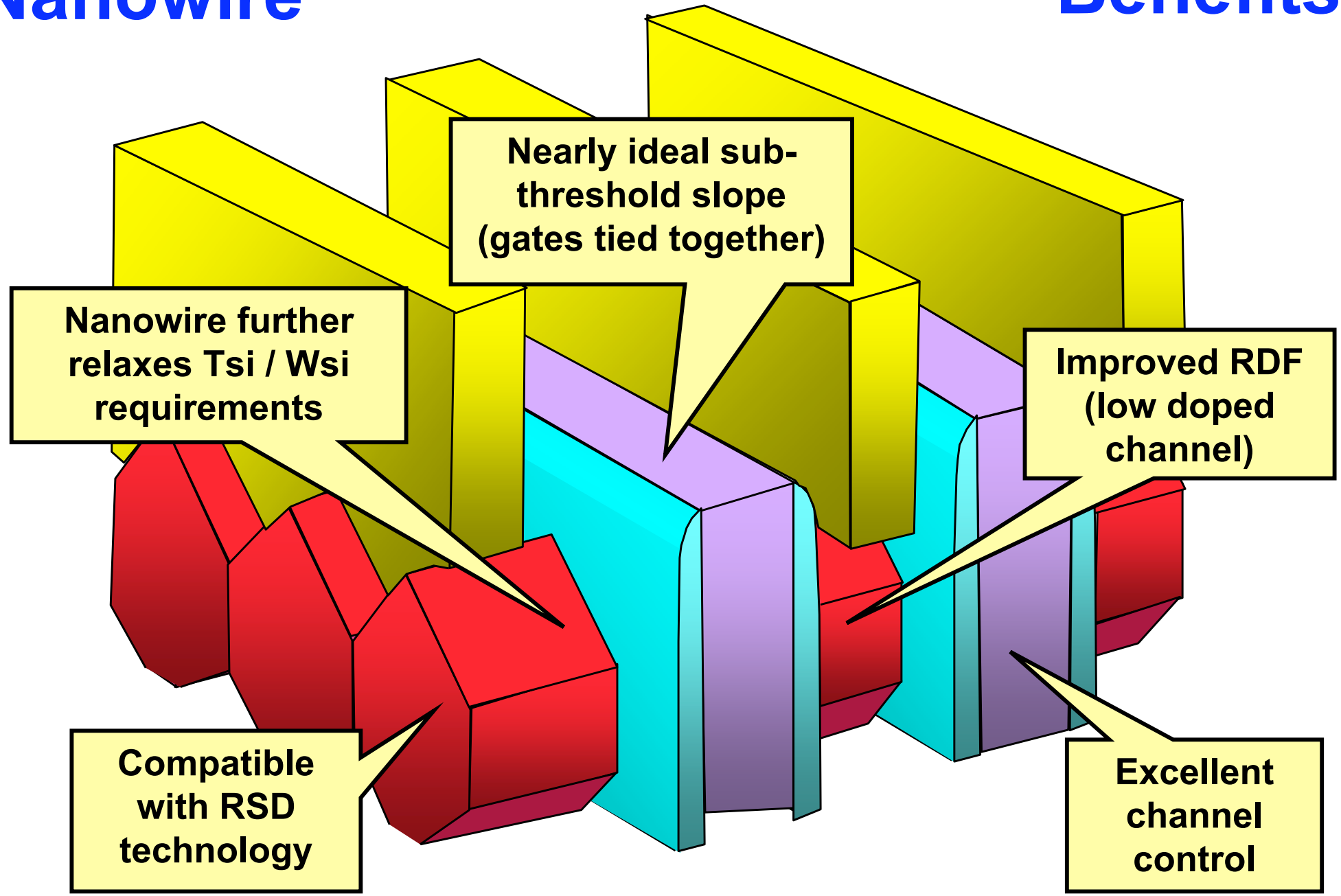




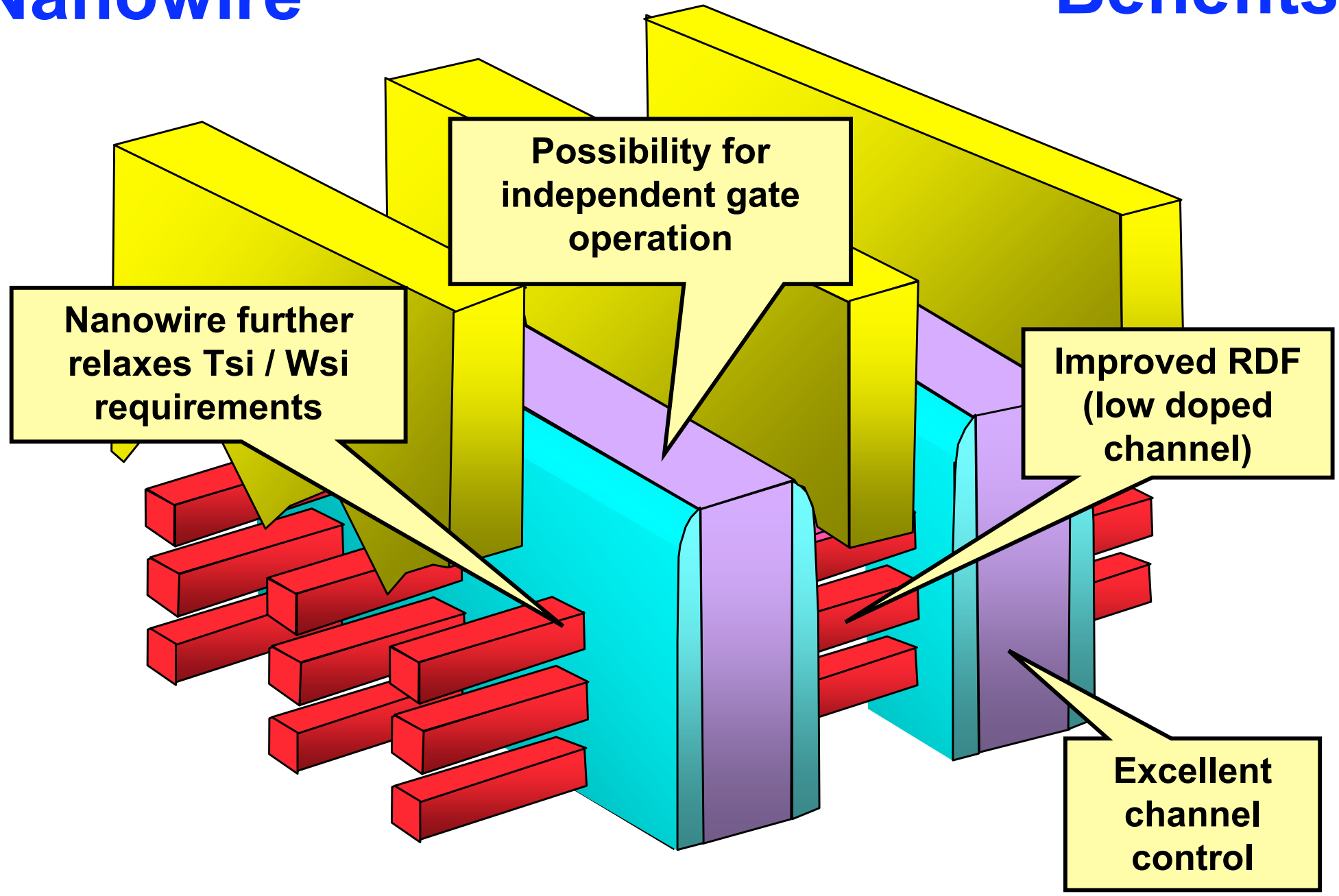
Nanowire Benefits



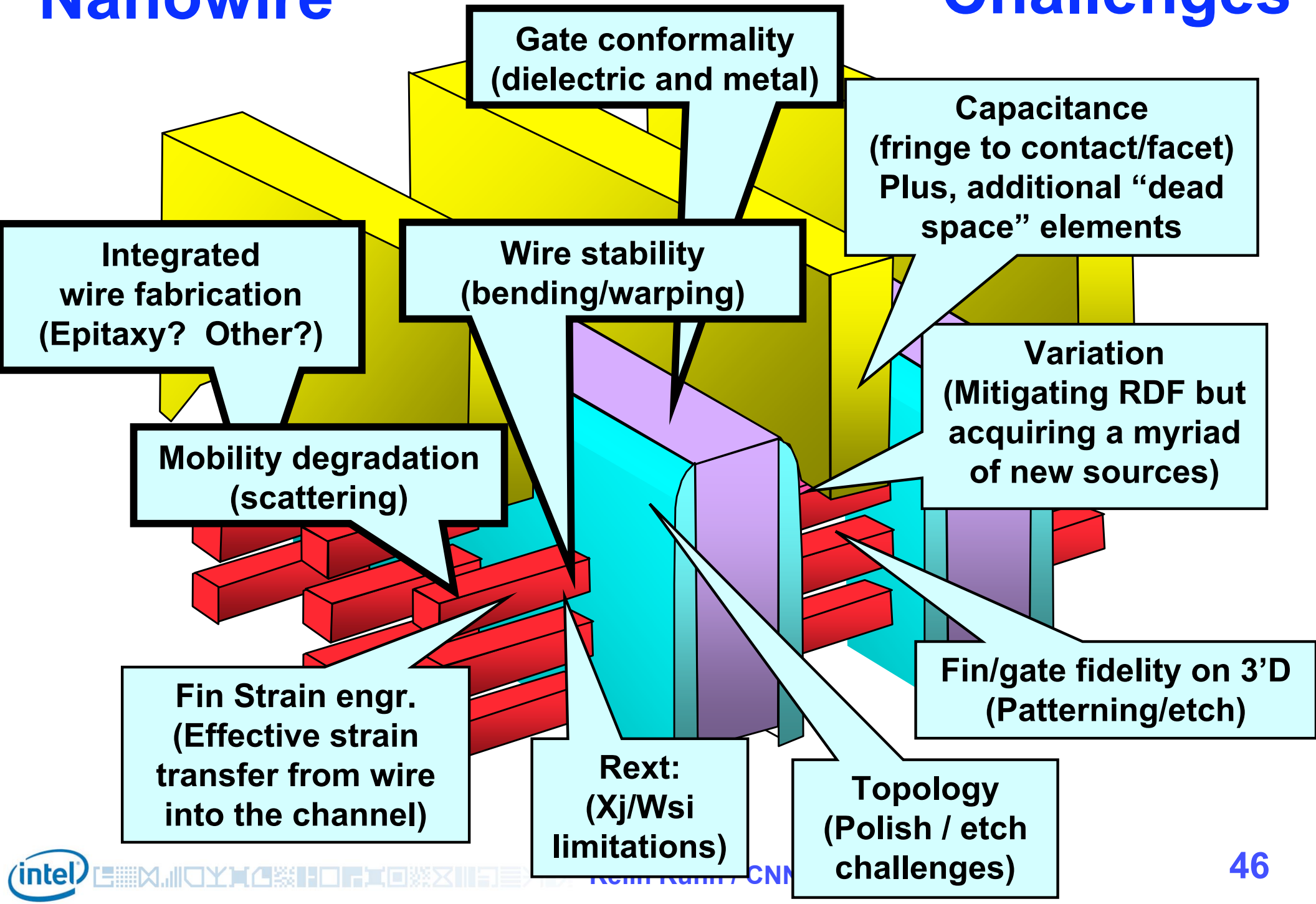
Nanowire Benefits



Nanowire Benefits

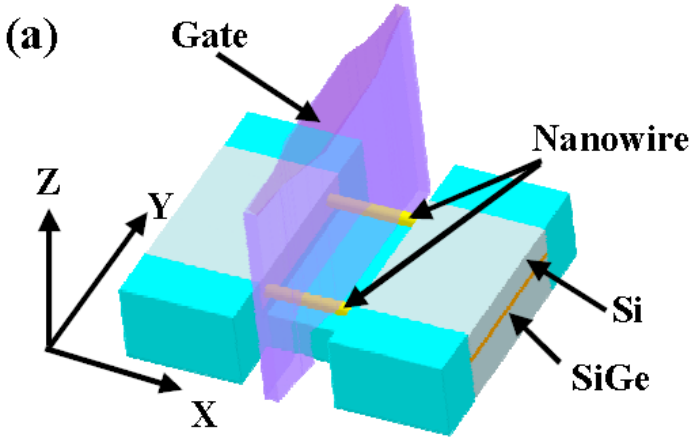


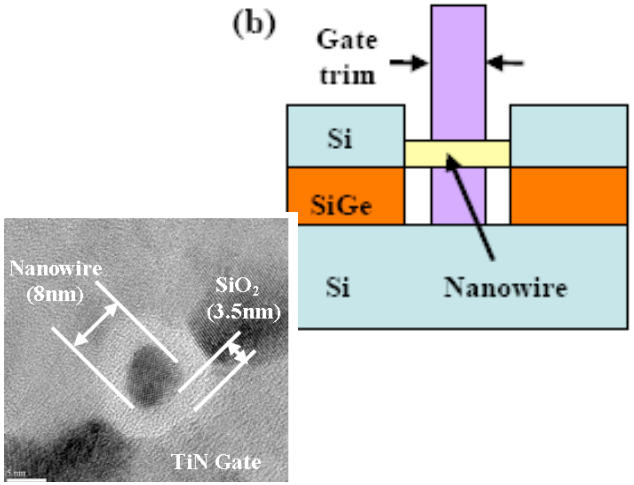
Nanowire Challenges

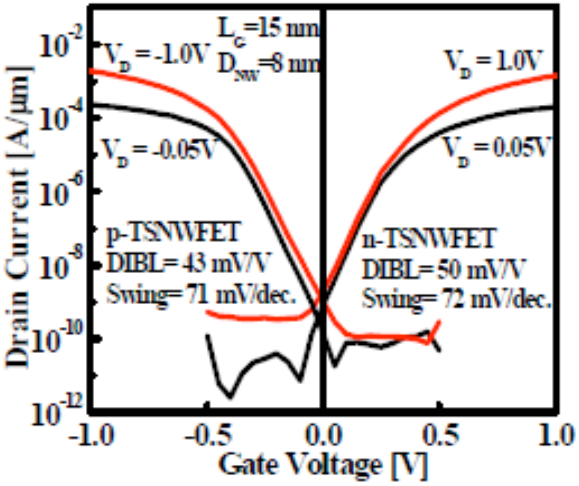


Nanowire FETs

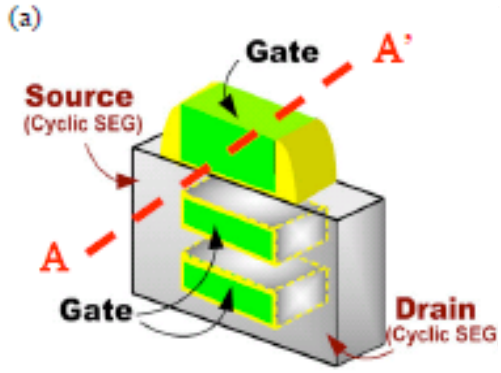
Yeo – Samsung – IEDM 2006

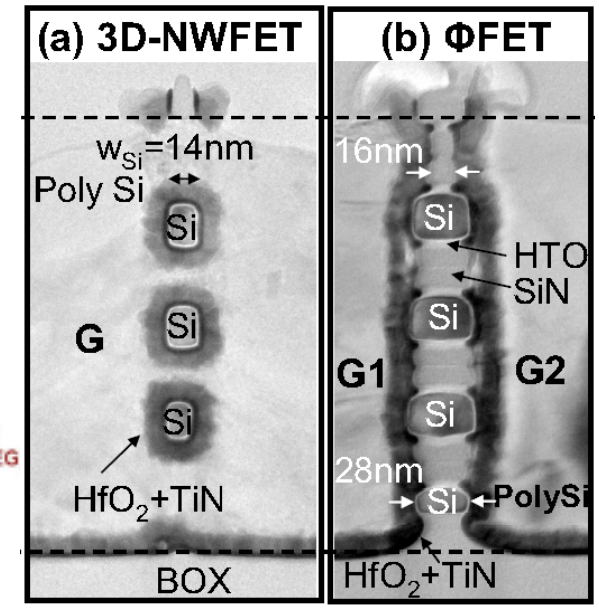


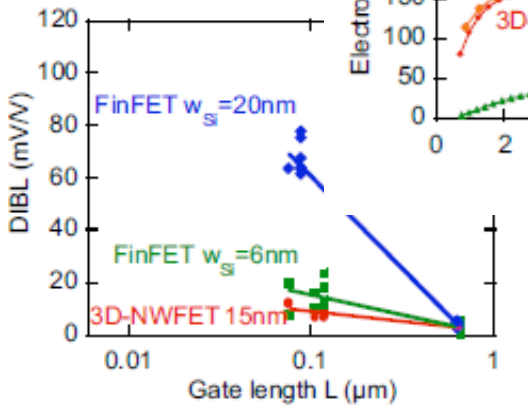


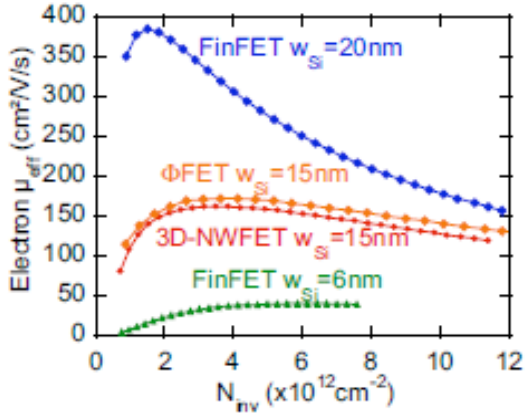


Dupre – CEA-LETI – IEDM 2008



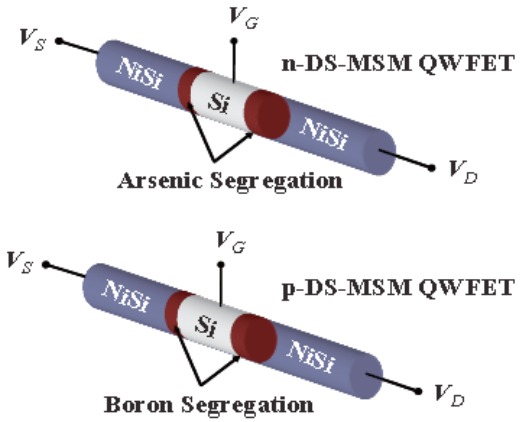


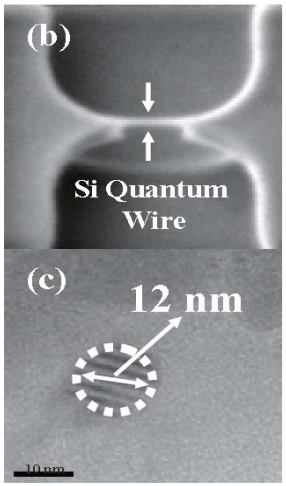


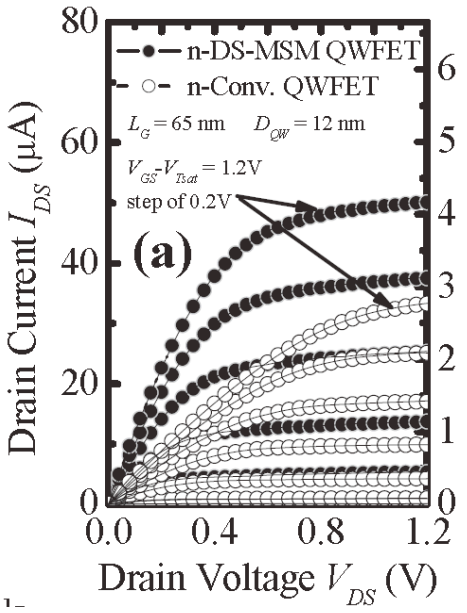


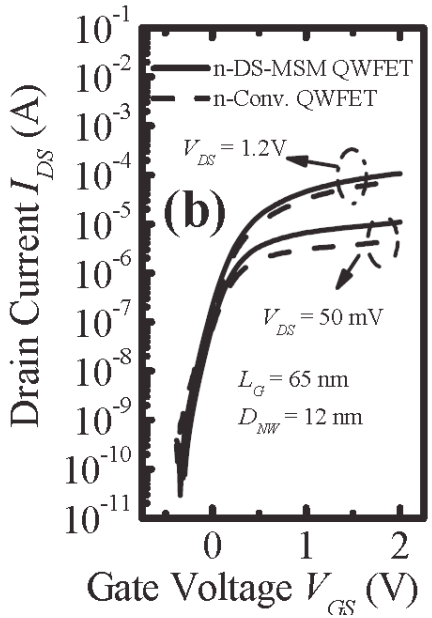
Nanowire FETs

Wong – NUS Singapore – VLSI 2009

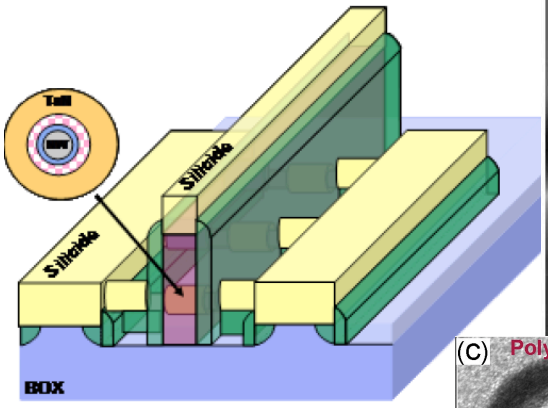


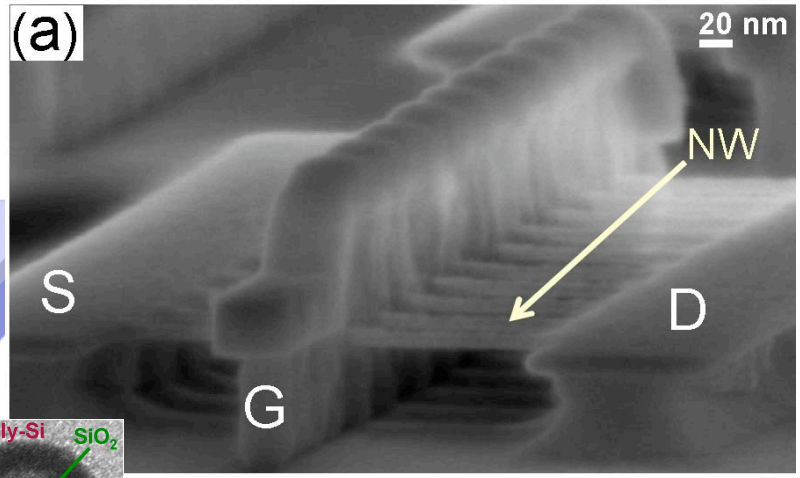


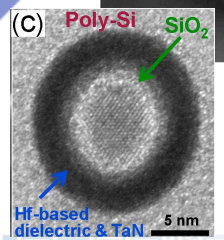


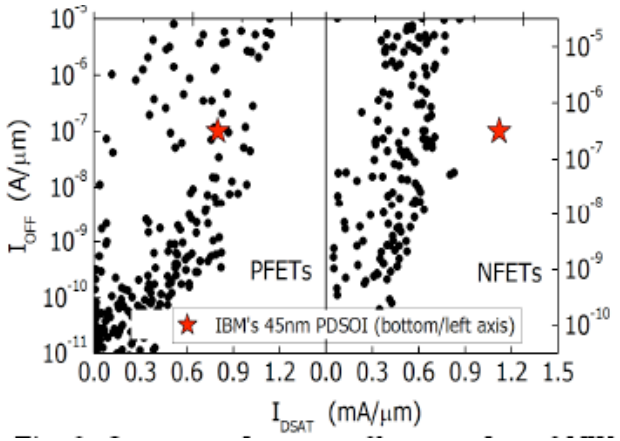


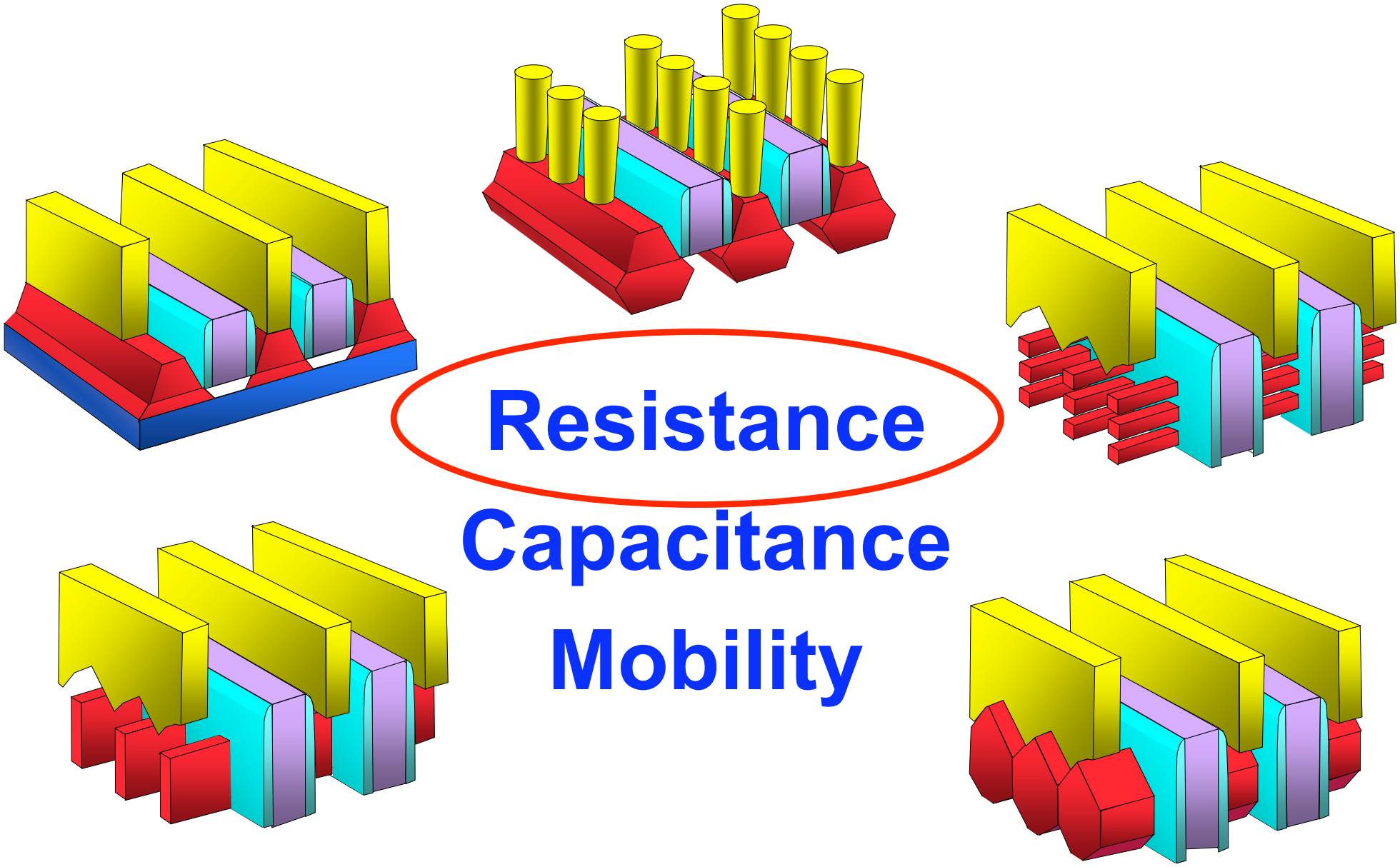
Bangsaruntip – IBM – IEDM 2009





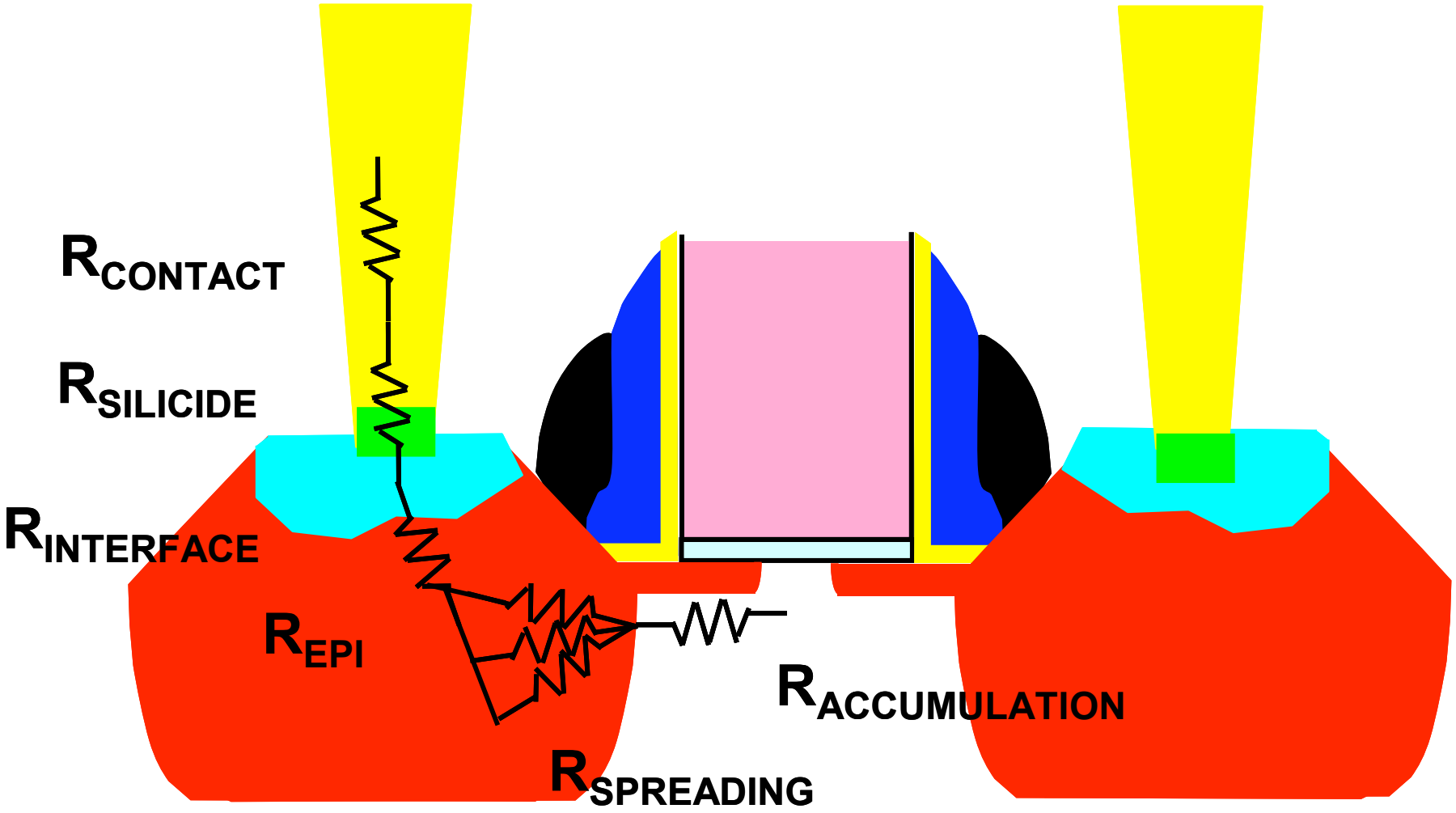




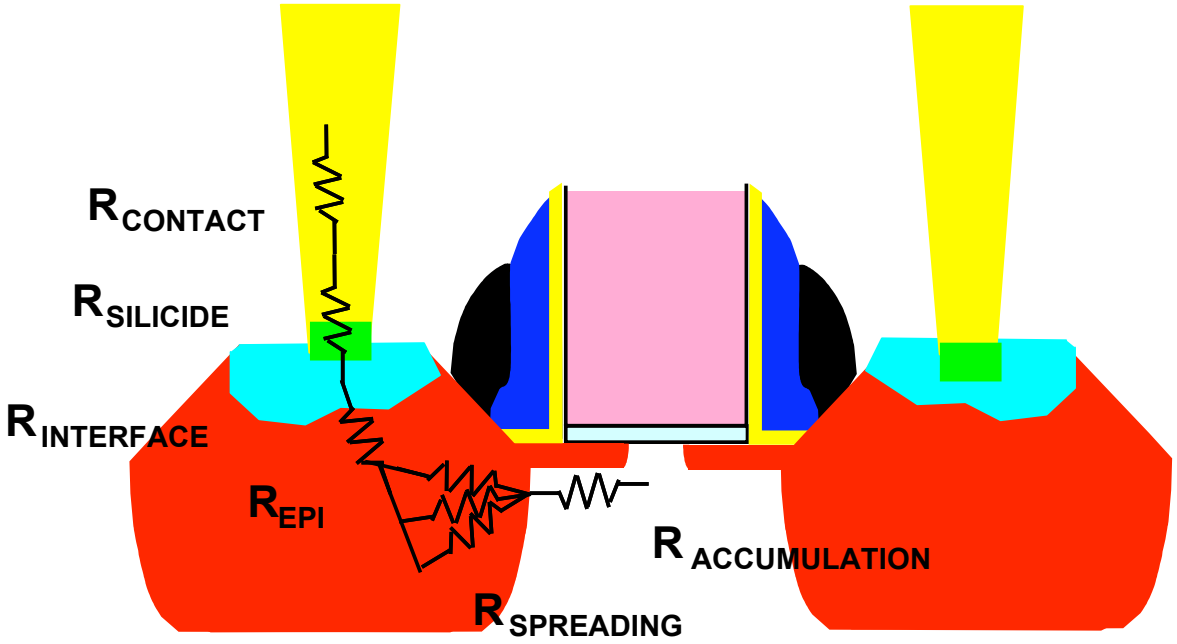


Challenges for ALL Architectures

Planar Resistive Elements



Improvement in Planar Elements



$$R_{\text{interface}} \propto \exp\left(\frac{q\phi_B}{\sqrt{N_D}}\right)$$

$$R_{\text{interface}} \propto \frac{1}{A}$$

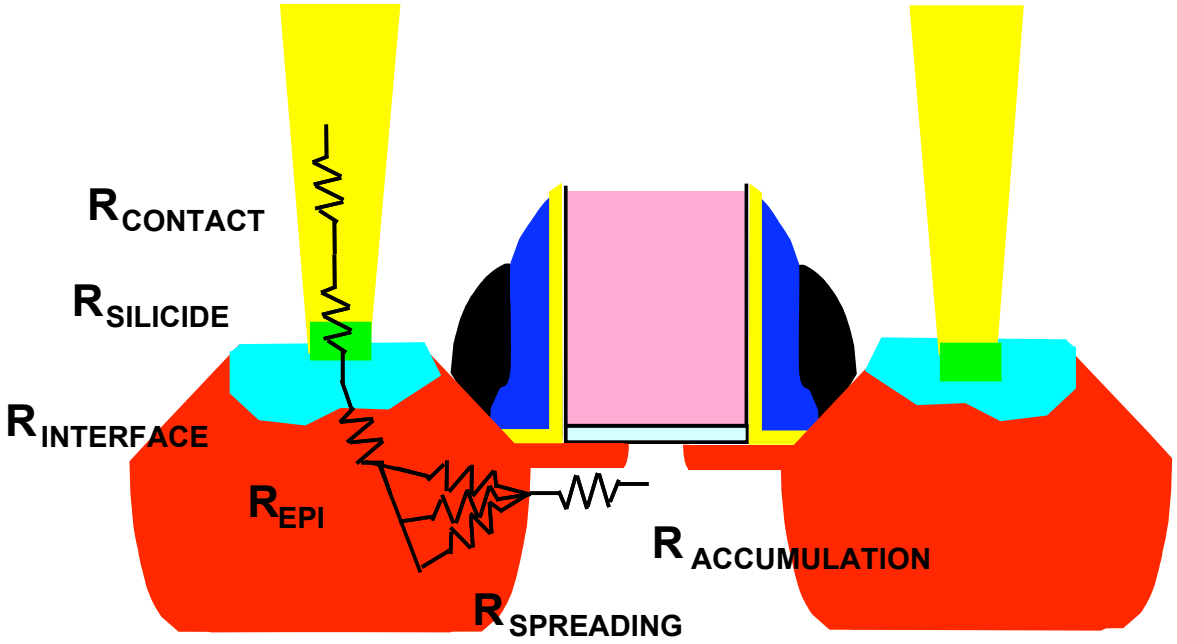
$q\phi_B - Schottky\ \ Barrier\ \ Height\ (SBH)$

$N_D - Substrate\ \ doping\ \ conc.$

$A - Contact\ \ area$

- Evolutionary R_{acc} improvement through X_j scaling (anneal/implant) until the end of the planar roadmap (thereafter Tsi/Wsi limited)
- R_{epi} / $R_{spreading}$ improvement from raised source/drain (RSD)
- Limited $R_{silicide}$ improvement (NiSi has the lowest known resistivity)
- Significant possibility for $R_{interface}$ improvement, particularly through SBH optimization ($R_{interface}$).
- $R_{contact}$ improvement from high conductivity metals (copper?)

Improvement in Planar Elements



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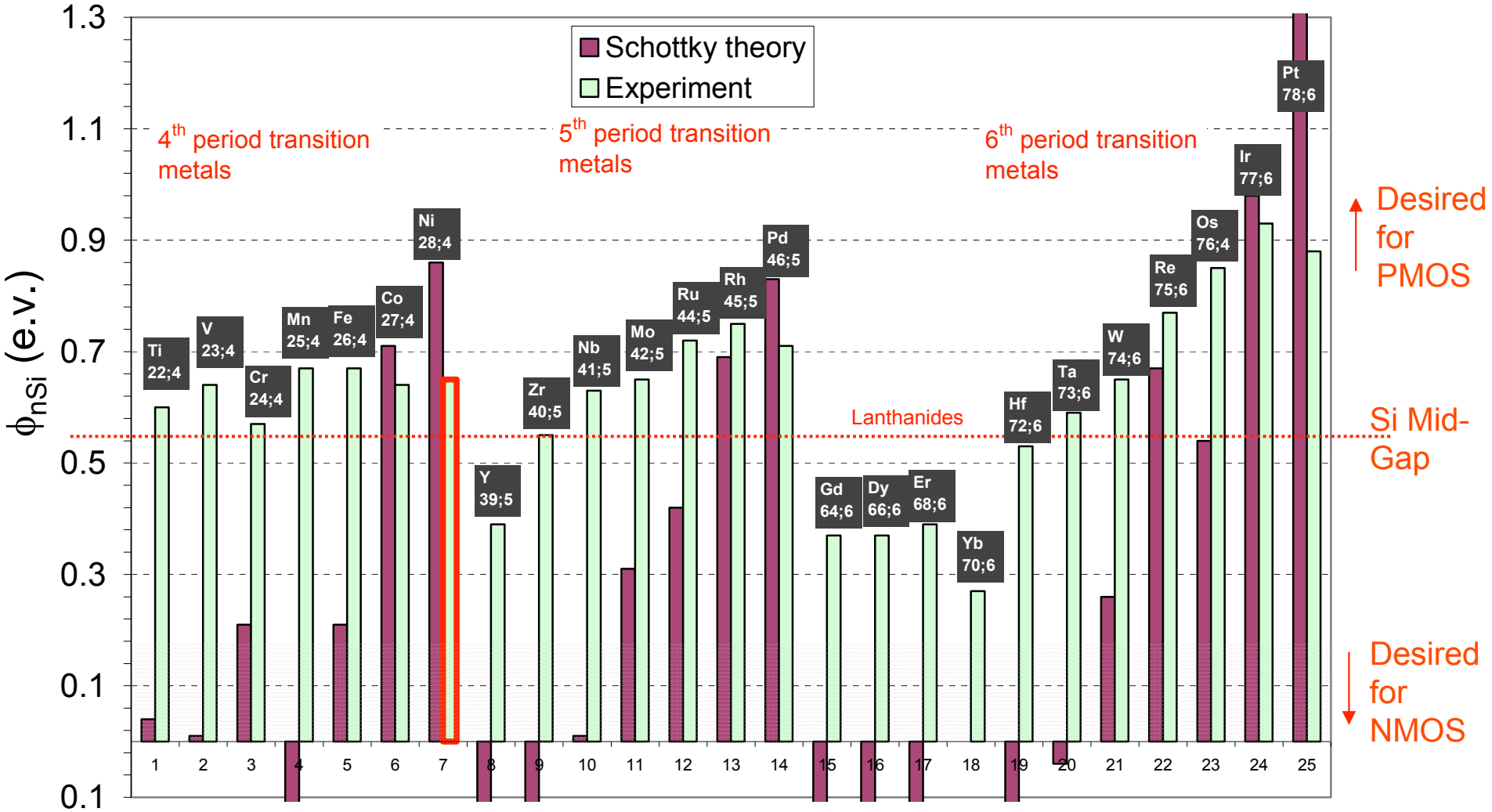
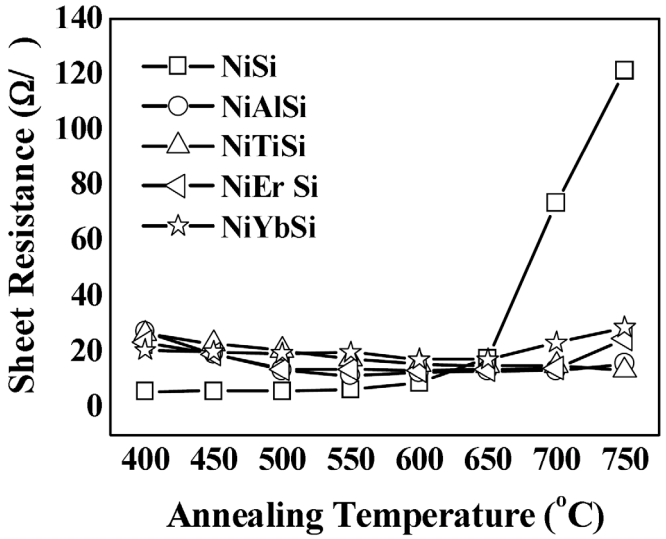
Schottky theory vs. experimental SBHs for metals on nSi
Mukherjee – Intel

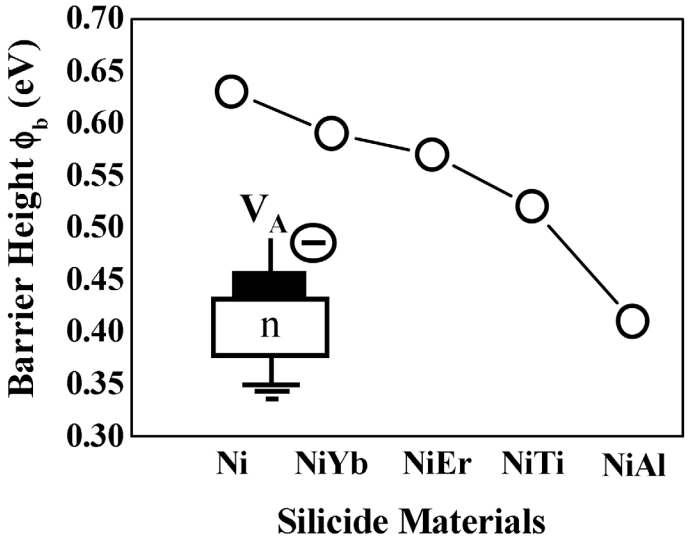


Fermi level pinned to mid-gap for most metals on Si

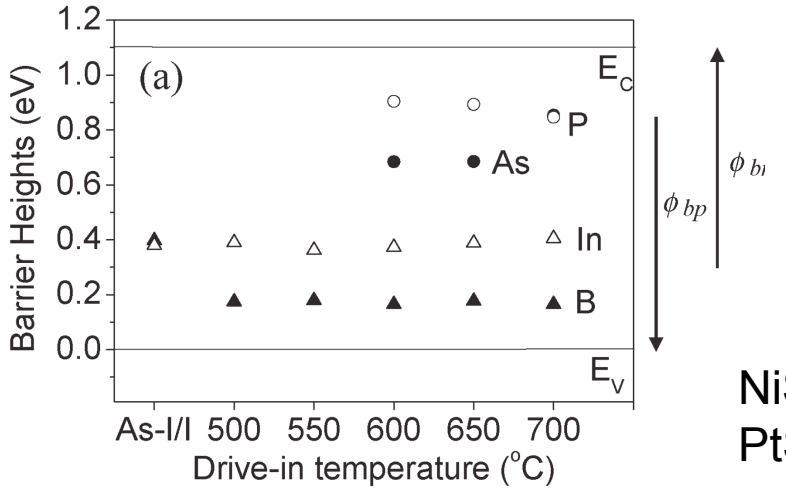
K. Kuhn – IEDM SC 2008

Alloy and Implant Modifications to Silicides

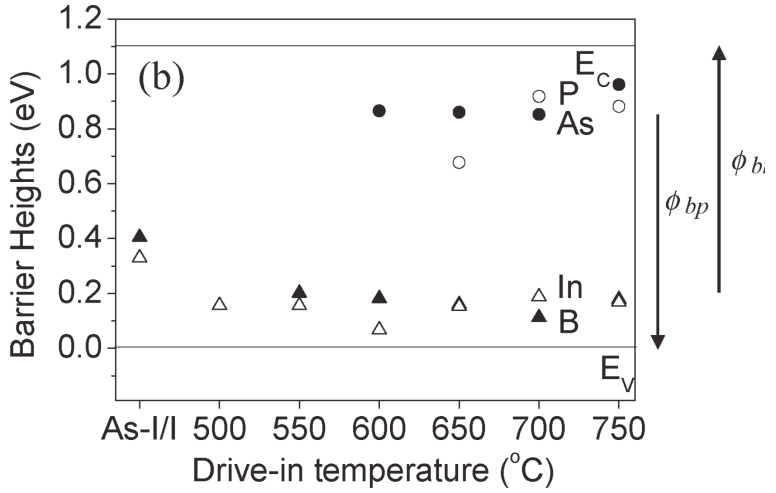




Lee –NUS-Singapore
IEDM 2006
Ni-alloy silicides

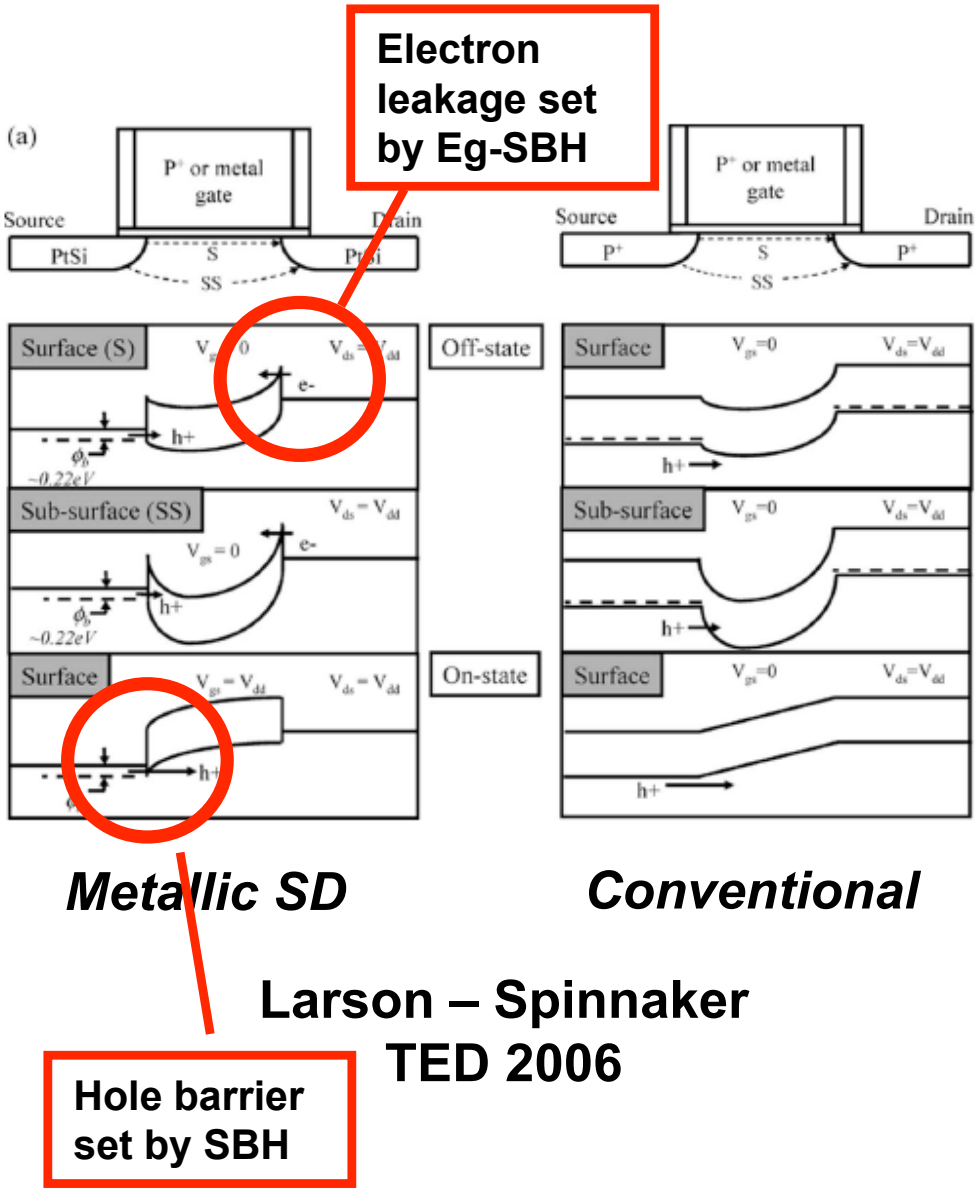


NiSi
PtSi



Zhang – KTH Sweden
EDL 2007
Implant modification of SBH
(SB FET paper)

Schottky barrier S/D – an option?



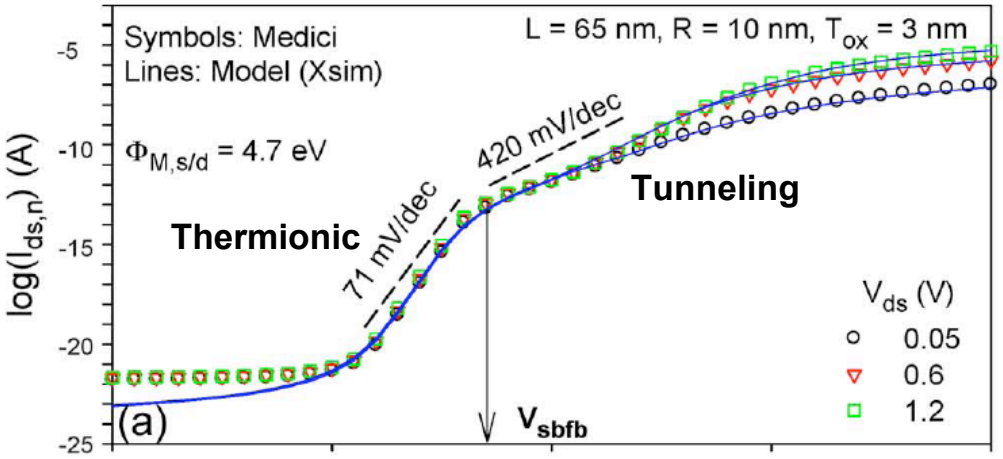
Larson – Spinnaker
TED 2006

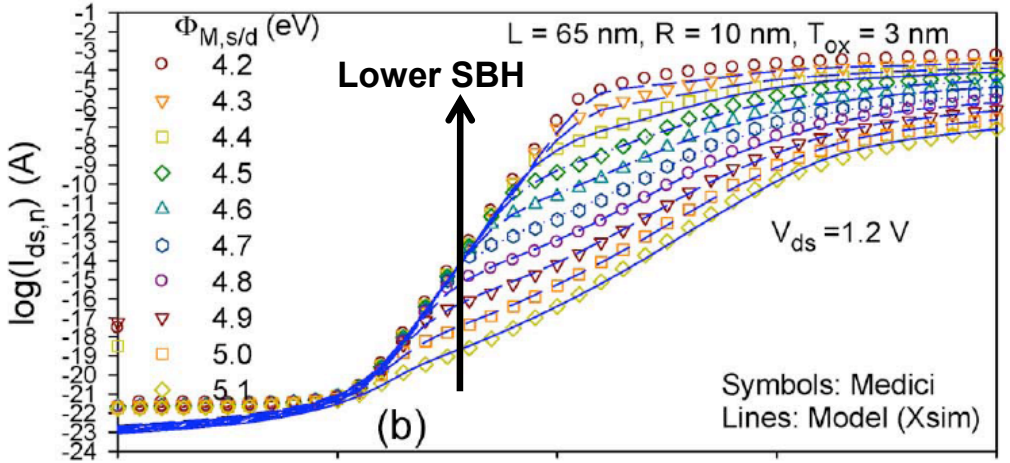
- In a metal SB-MOS, S/D forms an atomically abrupt Schottky-barrier having the height ϕb.
- The extreme limit for metal in the S/D regions (with associated improvements in Rext)
- Unconventional operation (field emission device in the ON state)
- Needs complementary devices (midgap silicide or two silicides)

Metal S/D Id-Vg Characteristics (Zhu)

Undoped nanowire

Zhu IEEE TED May 2009

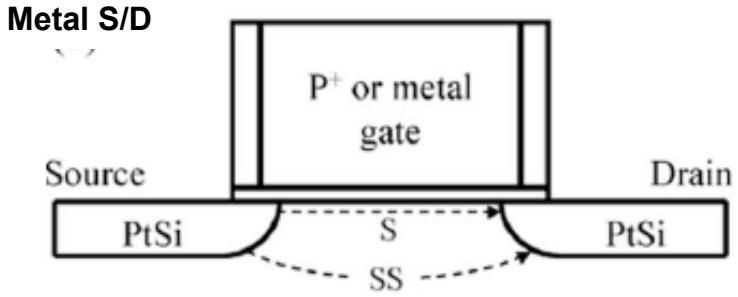


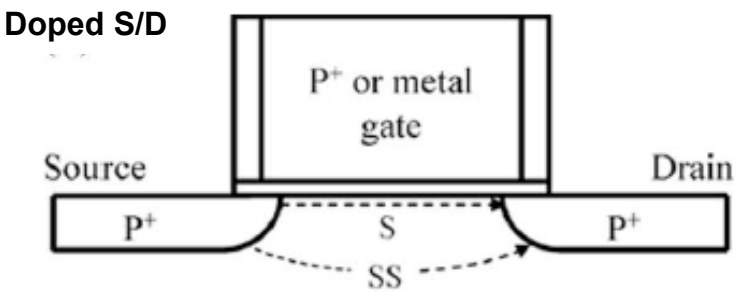


- Two possible conduction paths:
  - Thermionic – over the barrier – good subthreshold slope
  - Tunneling – through the barrier – poor subthreshold slope

- Two options to achieve thermionic control
  - Very low Schottky barrier height (<100meV)
  - Very heavy doping close to the barrier -> form thin doped s/d

Metal S/D – Benefits/Challenges



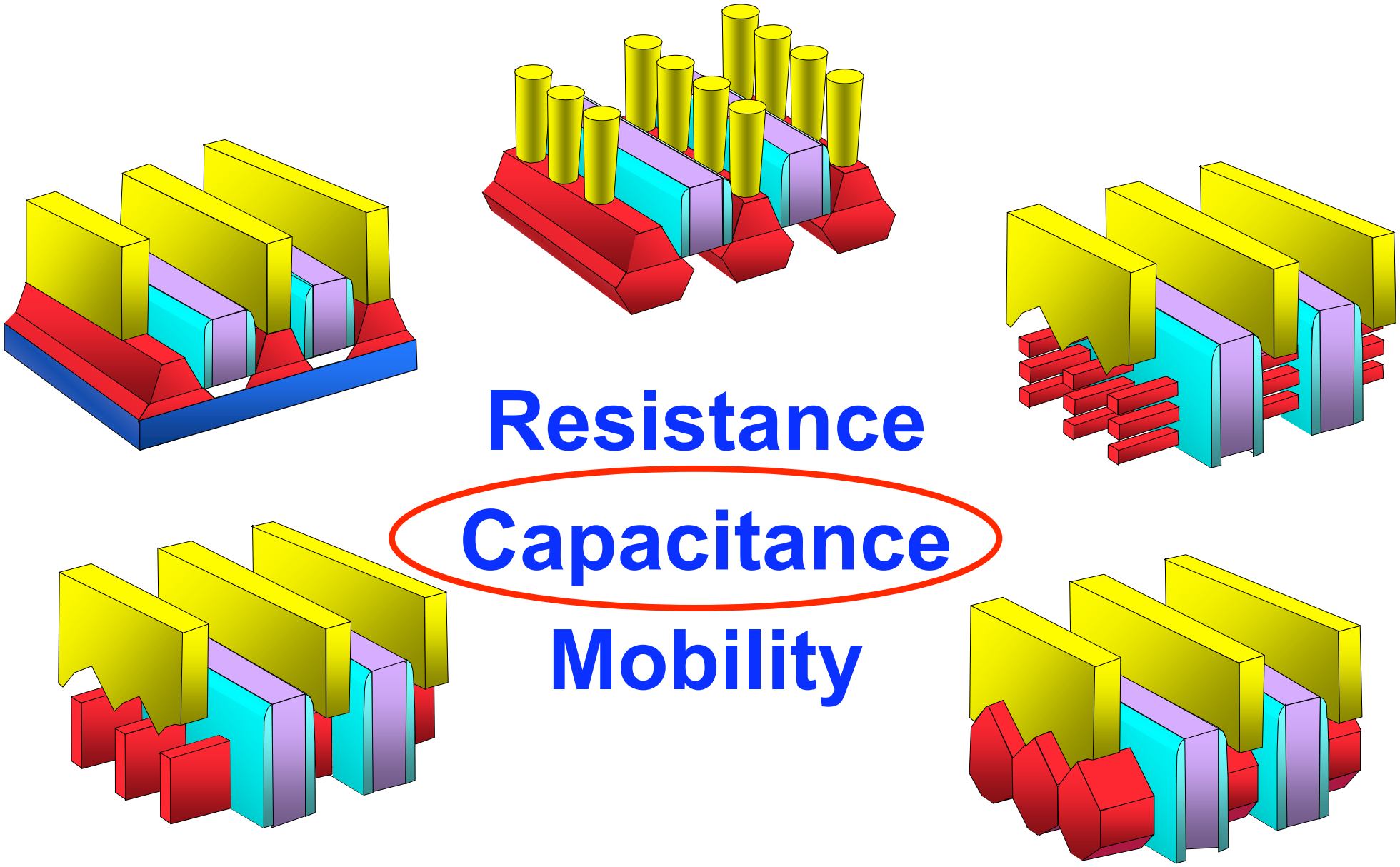


Benefits

- Low bulk resistance contacts to the channel
- Very abrupt junctions, allowing precise overlap/underlap
- No random s/d dopant fluctuation effects
- Minimize possible s/d carrier-carrier scattering effects with the channel

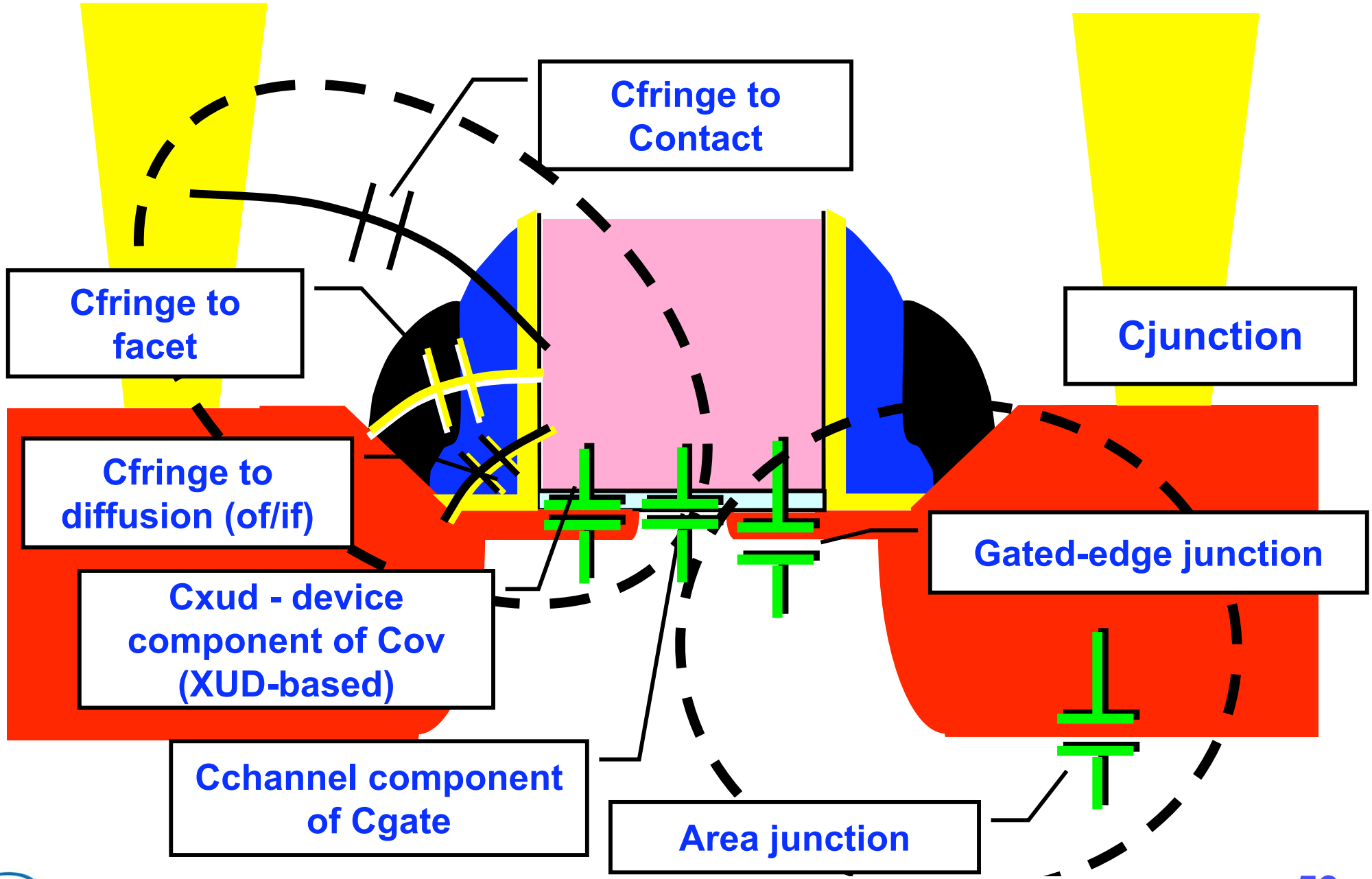
Challenges

- Poor experimental drive currents
- Requires very low Schottky barriers, low resistance interfaces
- Ambipolar conduction (high drain-body leakage for bulk devices)
- Early contact formation limits midsection process temperatures
- Need alternative approach for s/d stressors

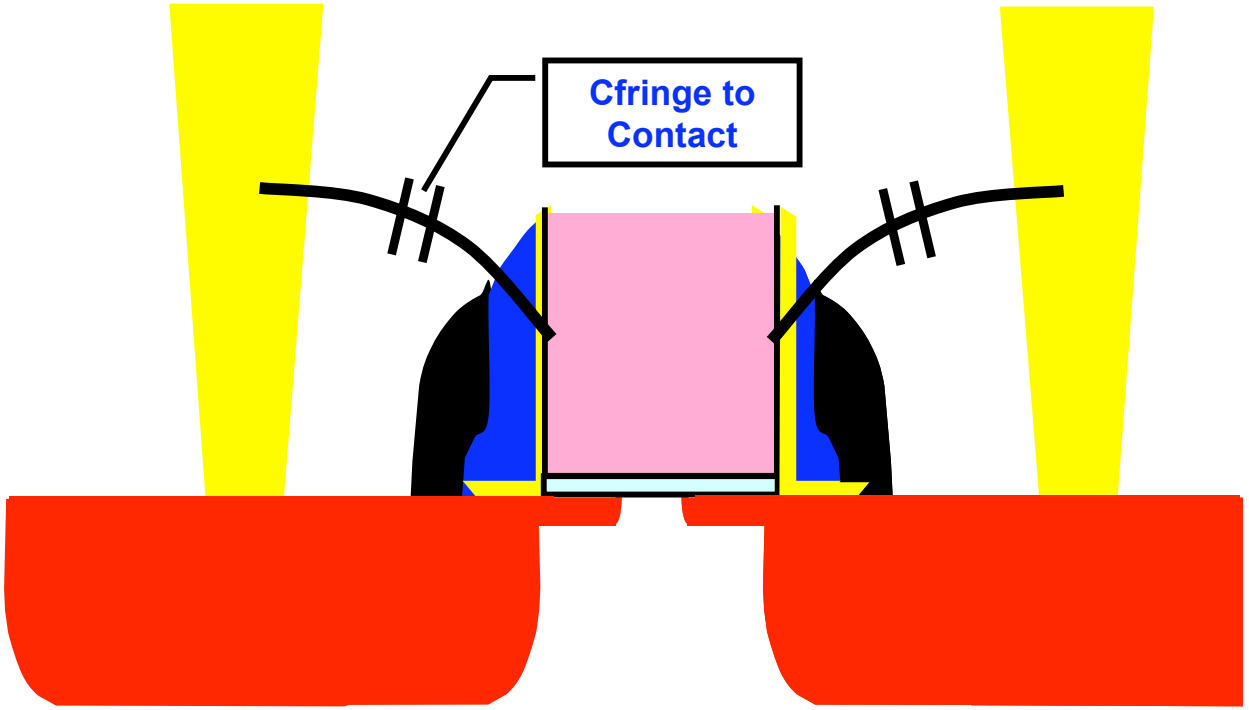


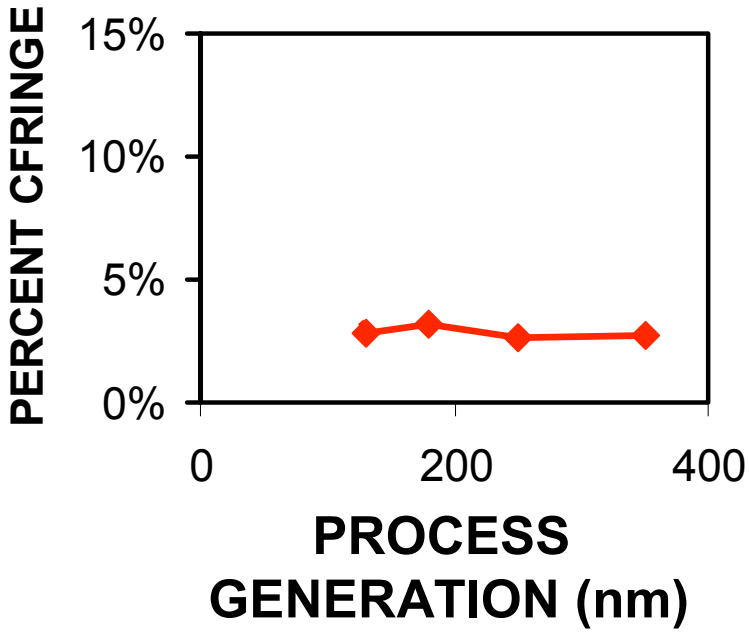
Challenges for ALL Architectures

Planar Capacitive Elements



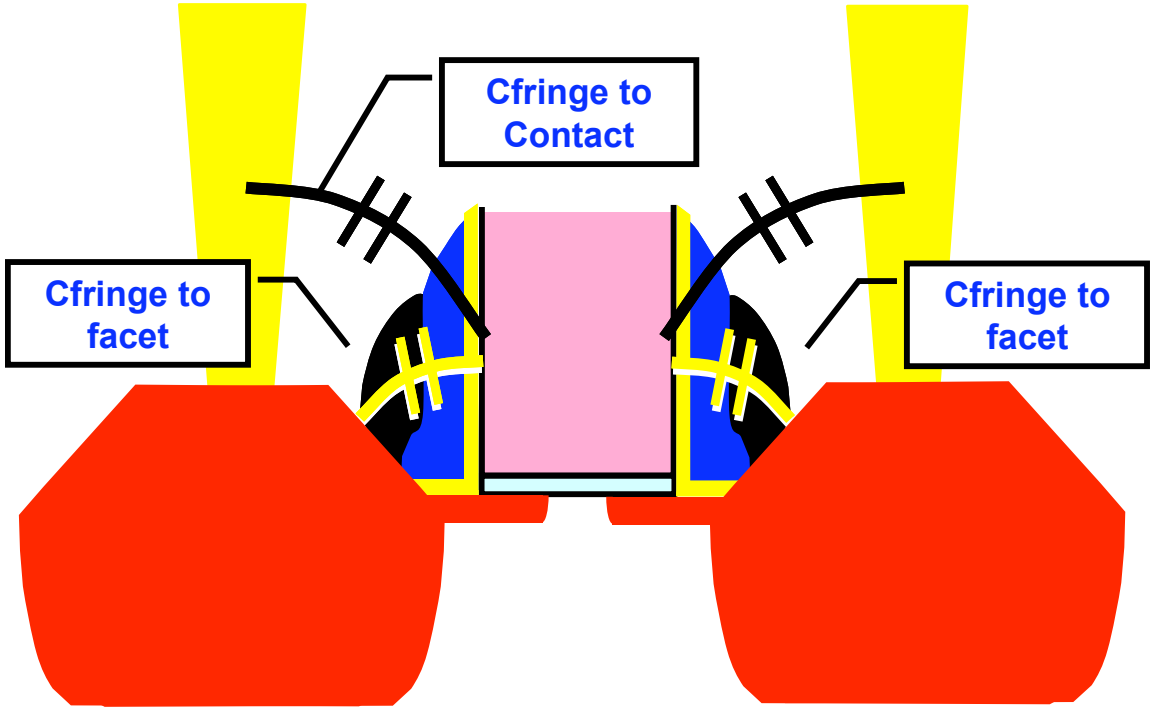
Planar Capacitive Elements

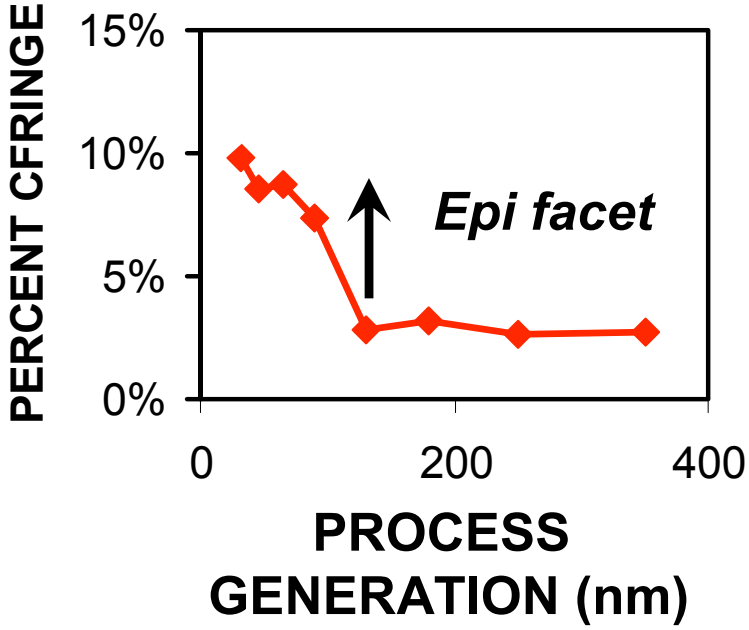




"Golden" days of scaling:
Who worried about Cfringe?

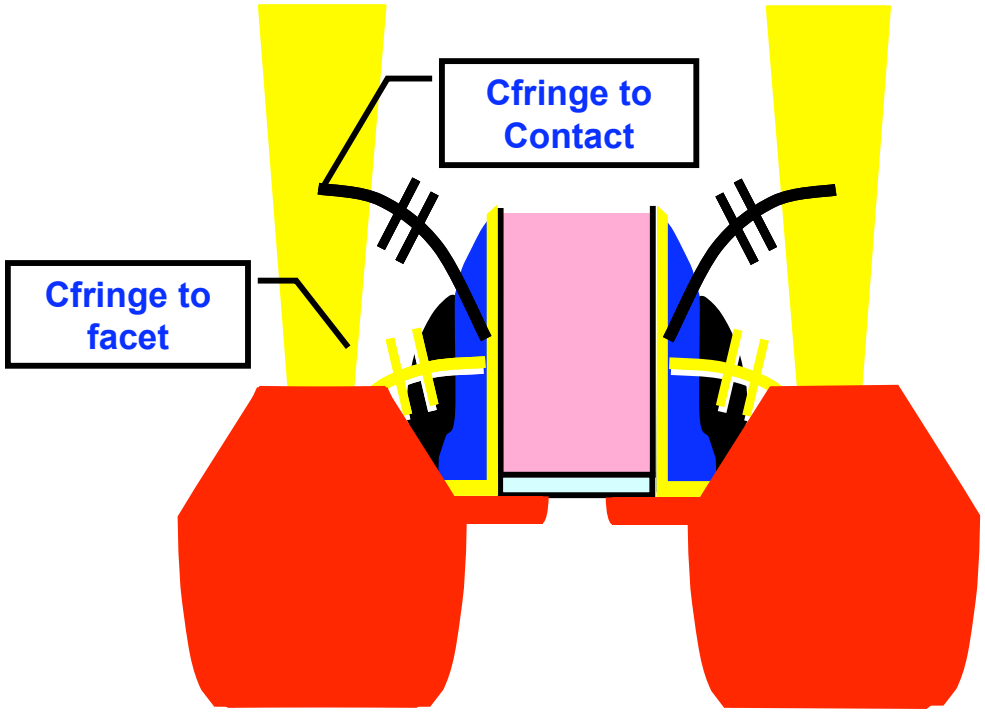
Planar Capacitive Elements

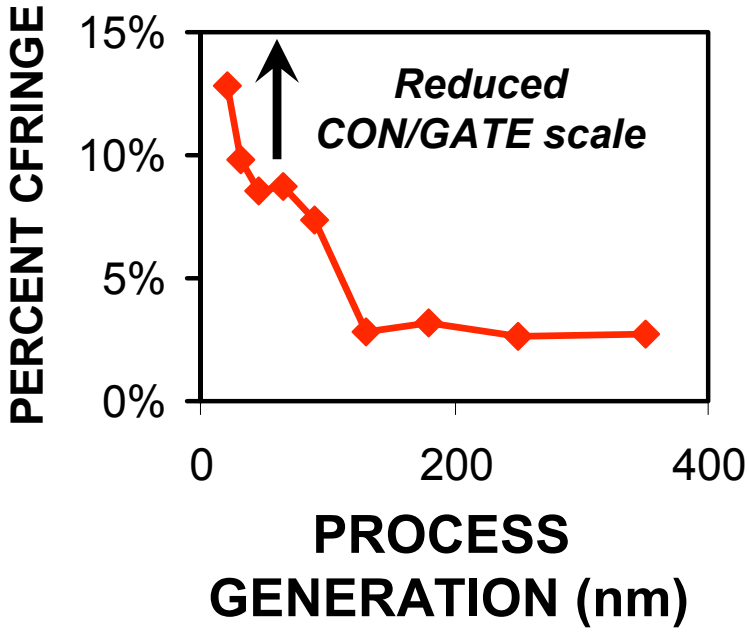




"Silver" days of scaling: Introduction of epi: Increased fringe due to facet

Planar Capacitive Elements

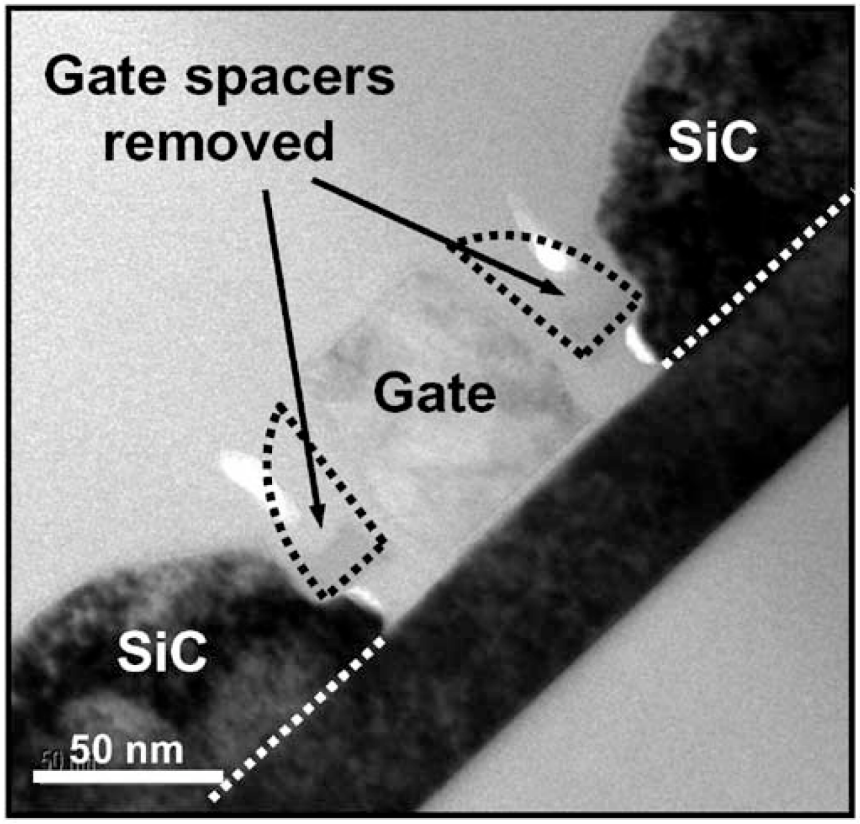




"Bronze" days of scaling

Gate and contact CD dimensions scaling slower than contacted gate pitch – fringe matters

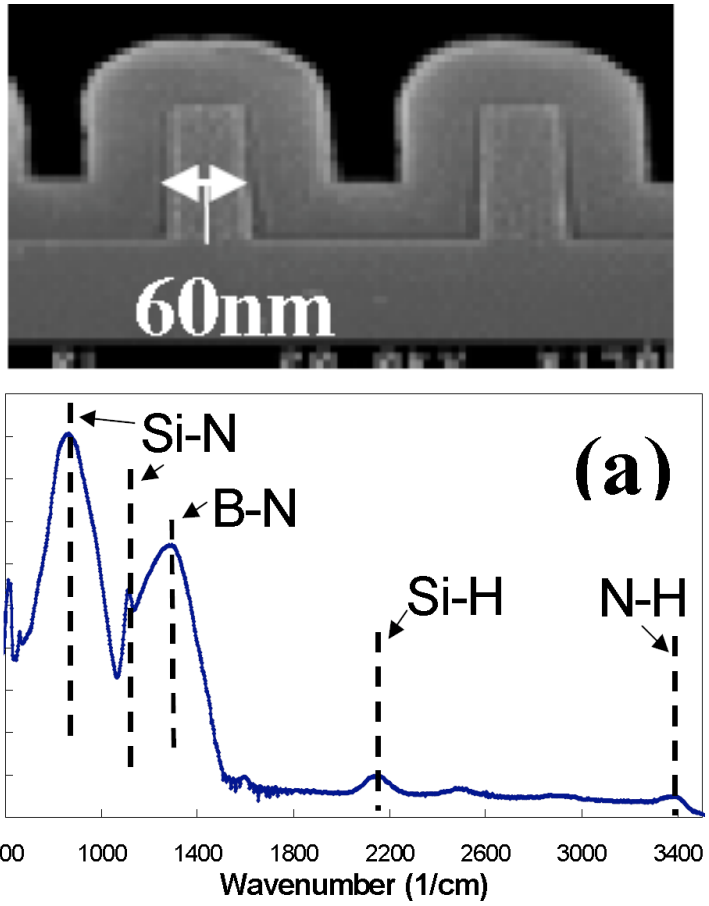
Innovative Spacer Technologies



SPACER REMOVAL

Liow – NUS Singapore

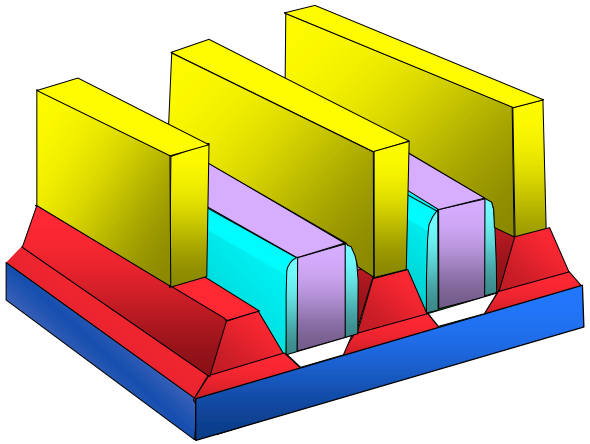
EDL 2008

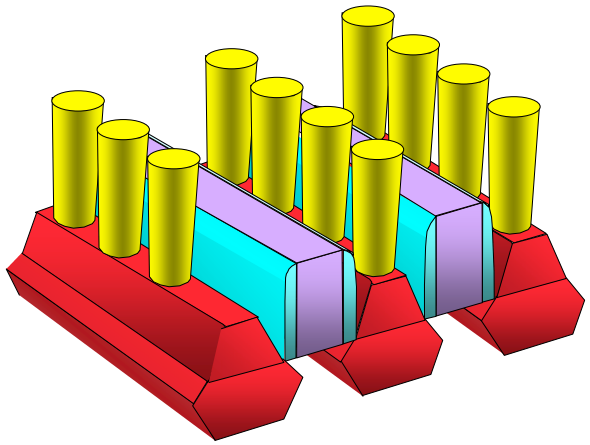


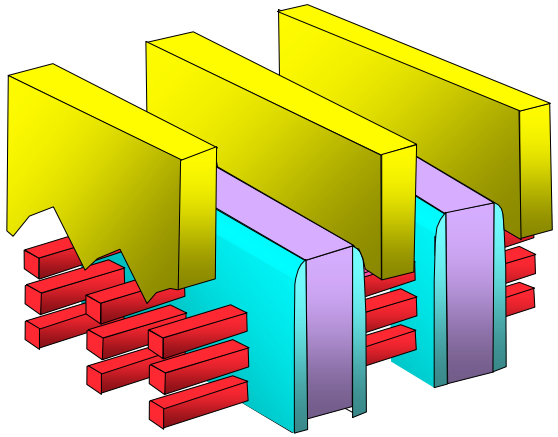
SiBCN (Low-K) SPACER

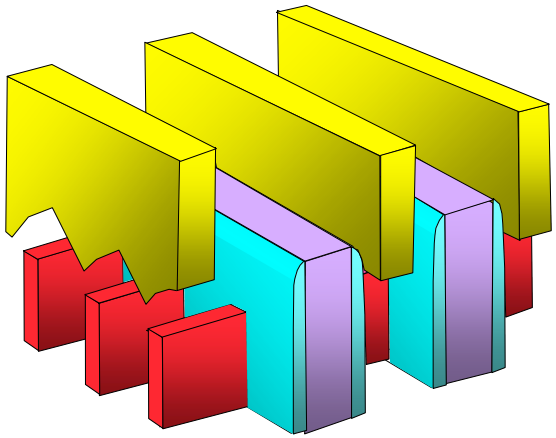
Ko –TSMC

VLSI 2008

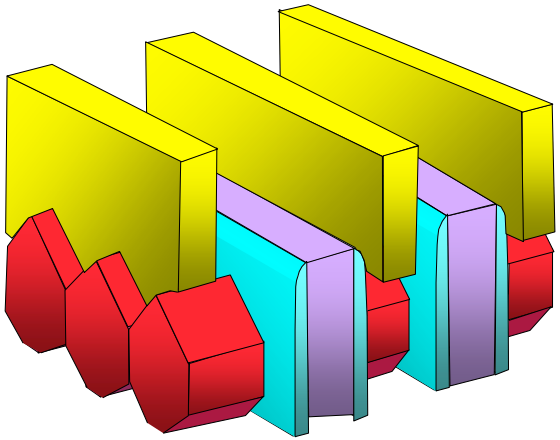






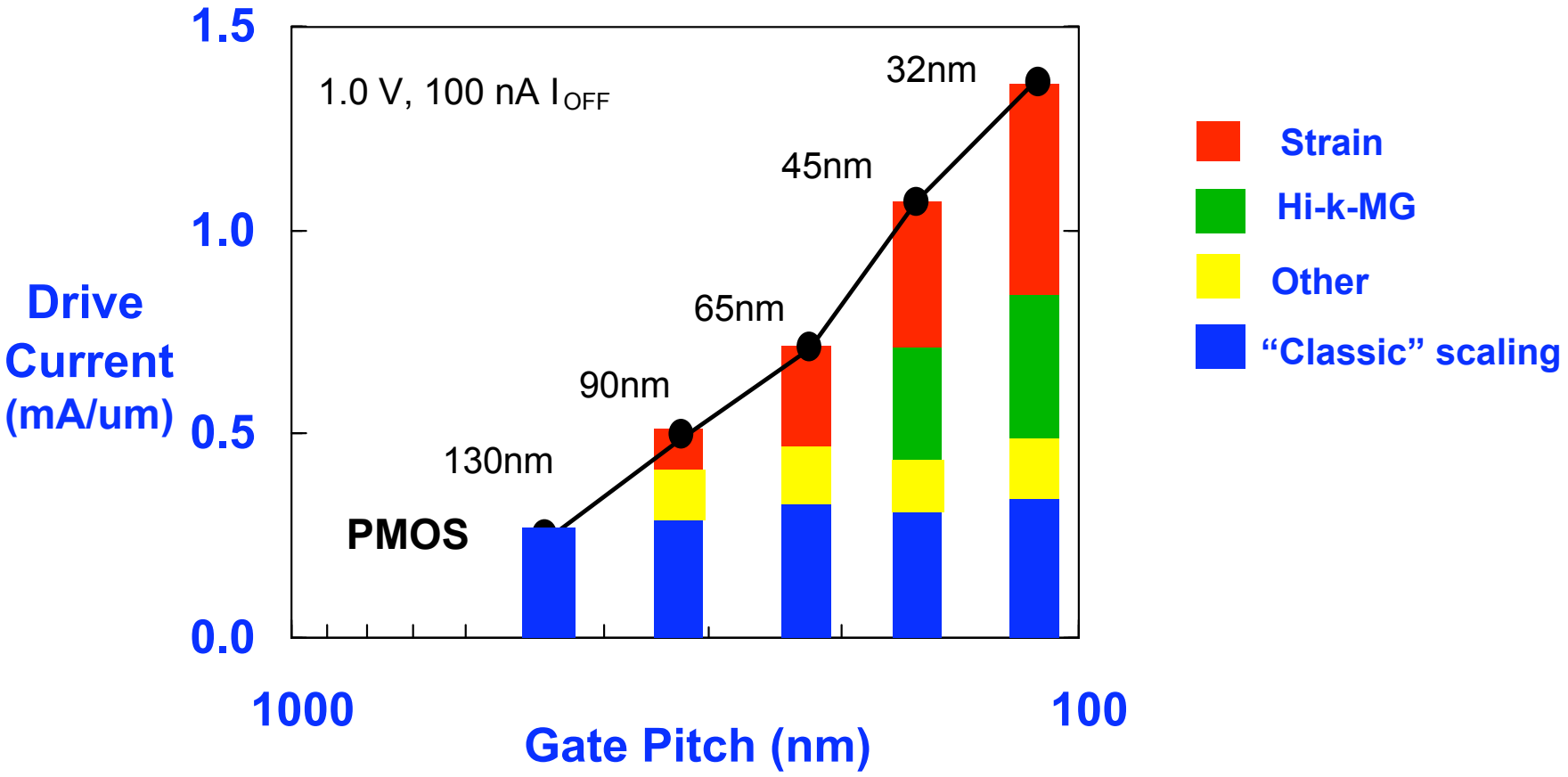


Resistance
Capacitance
Mobility



Challenges for ALL Architectures

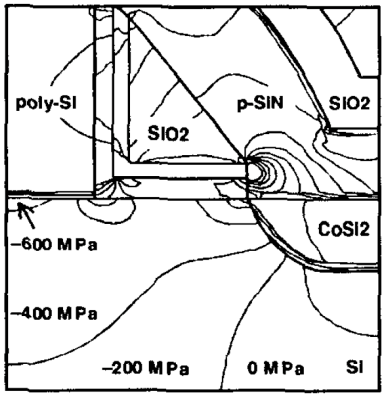
Transistor Performance Trend

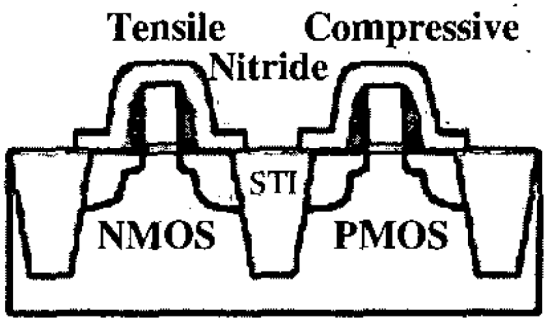


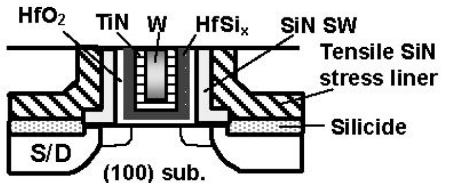
Strain is a critical ingredient in modern transistor scaling

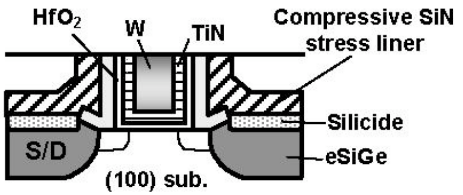
Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation

Etch-stop nitride (CESL)

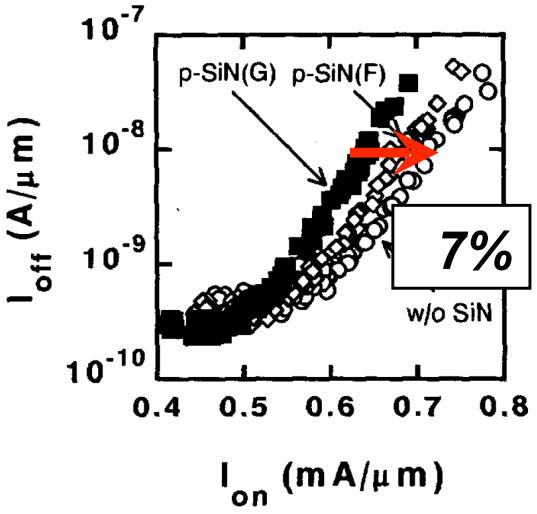


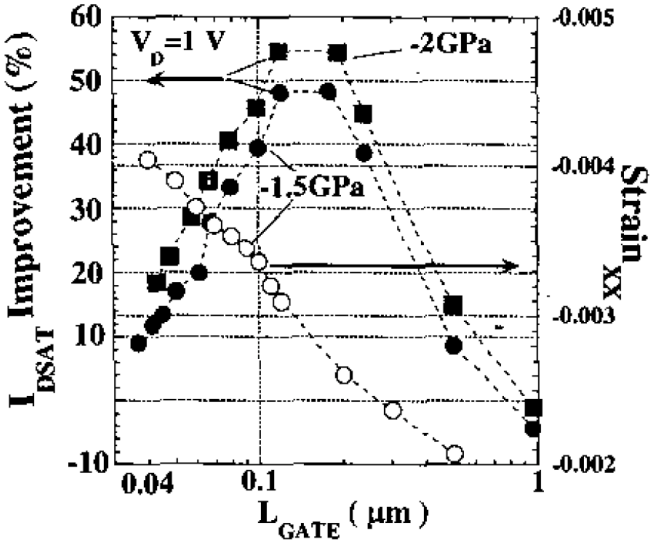


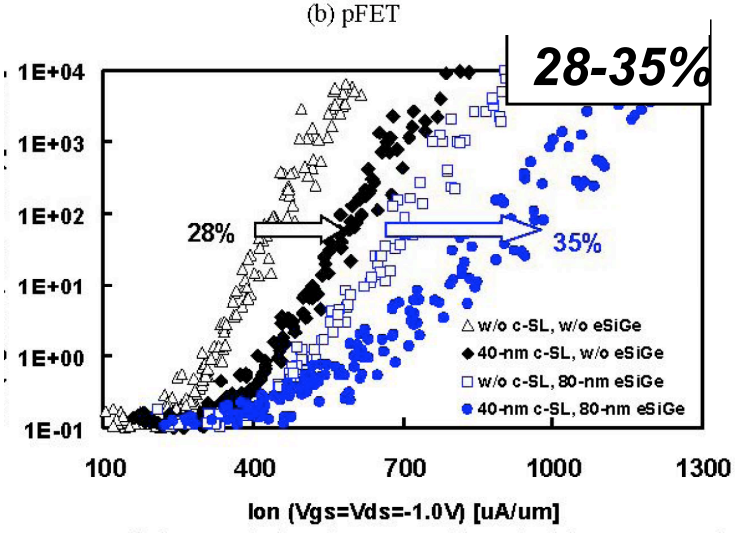




(b) pFET





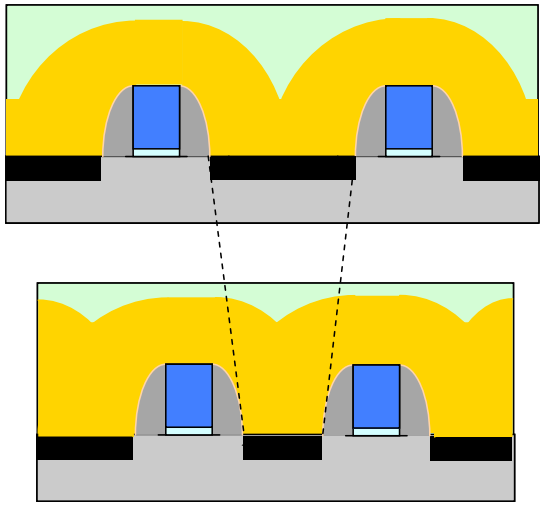


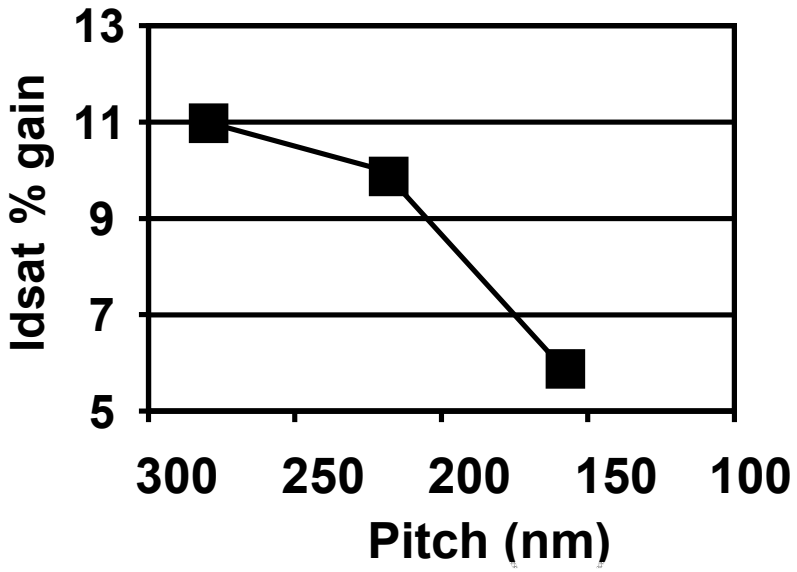
Ito – NEC
IEDM 2000
NMOS SiN strain

Pidin – Fujitsu
IEDM 2004
N and PMOS

Mayuzumi – Sony
IEDM 2007
Dual-cut stress liners
(MG process)

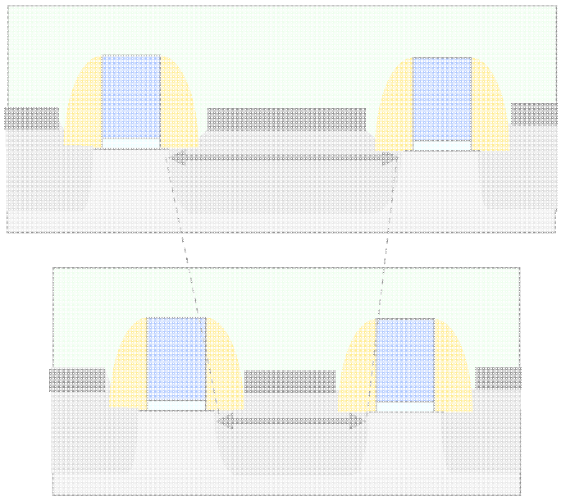
Strain: Pitch dependence

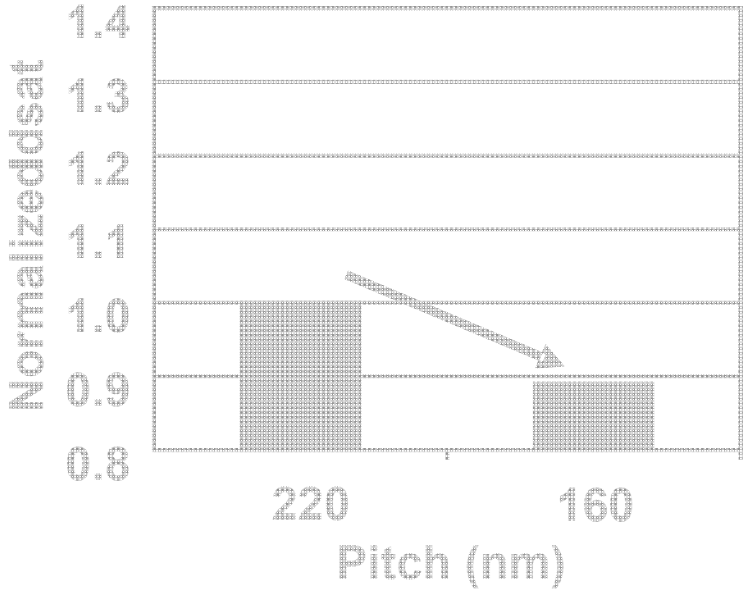




NMOS

Pitch degradation increases with film pinchoff, requires higher stress, thinner films



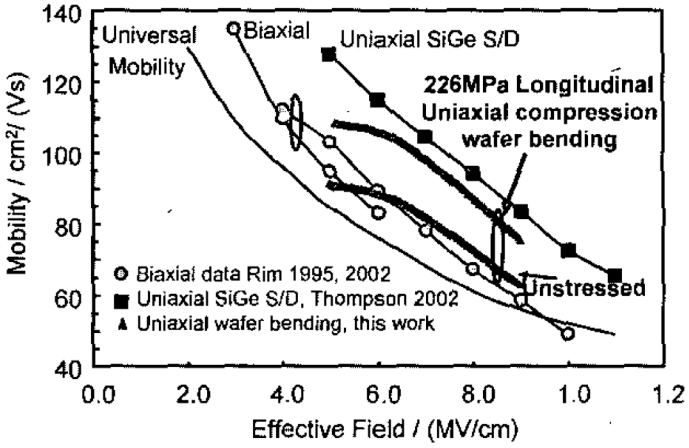


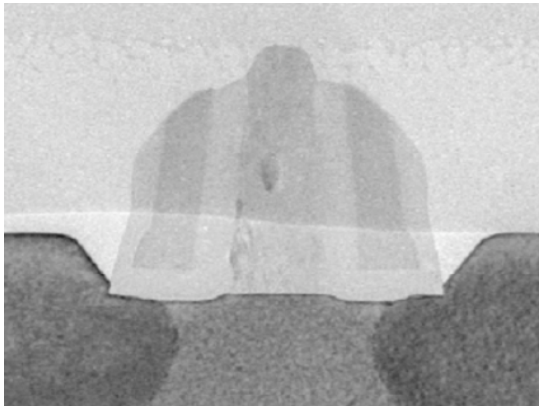
PMOS

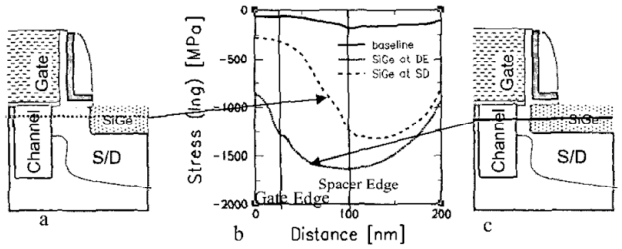
eSiGe S/D mobility strongly dependent on pitch

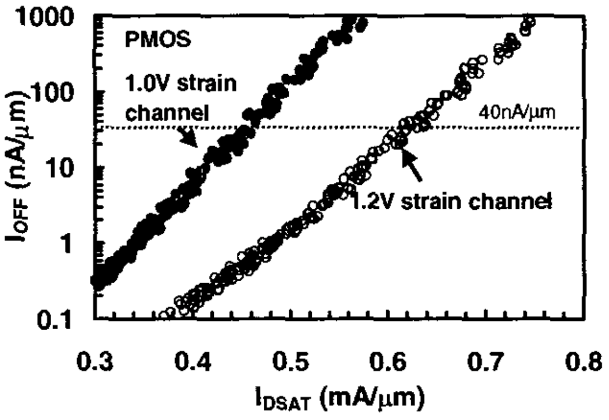
Auth, Intel, VLSI 2008

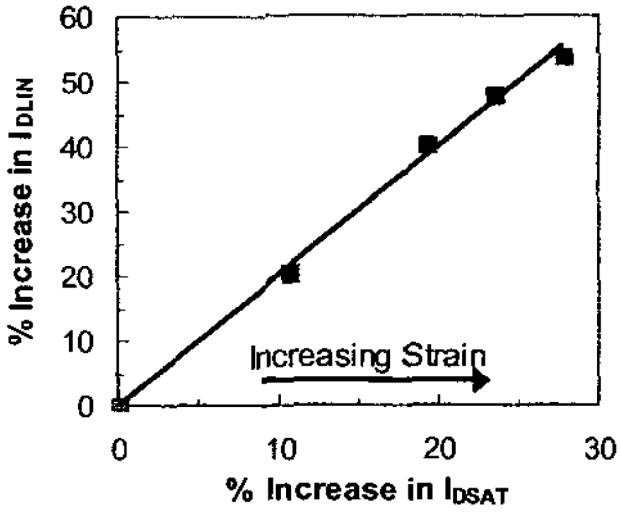
Embedded SiGe (PMOS)

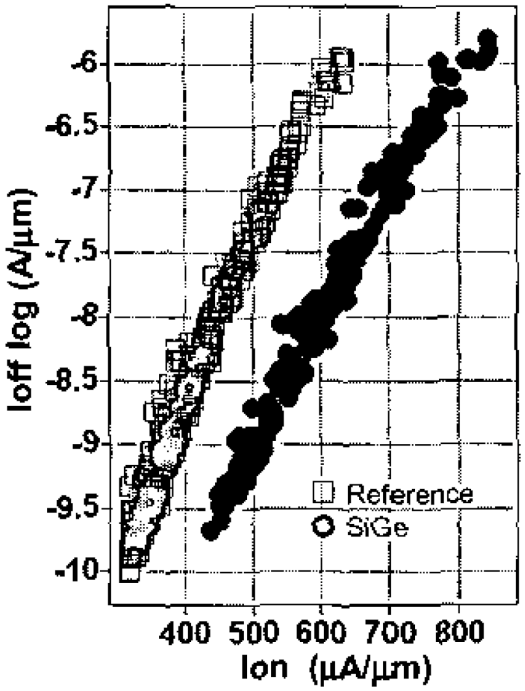










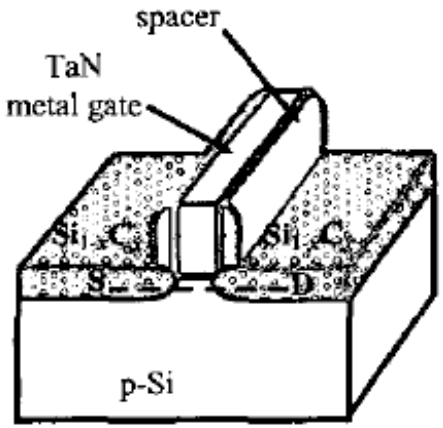


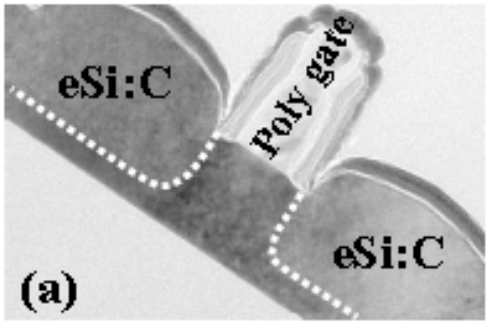
Thompson – Intel
IEDM 2002 / 2004

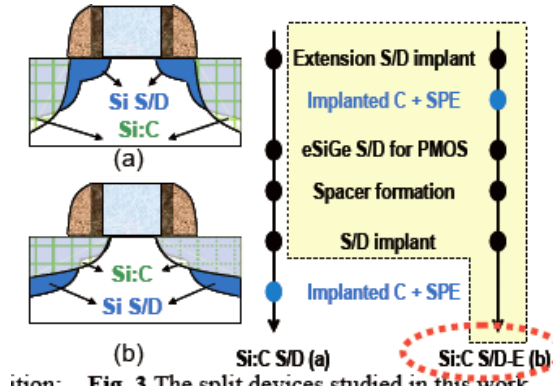
Ghani – Intel
IEDM 2003

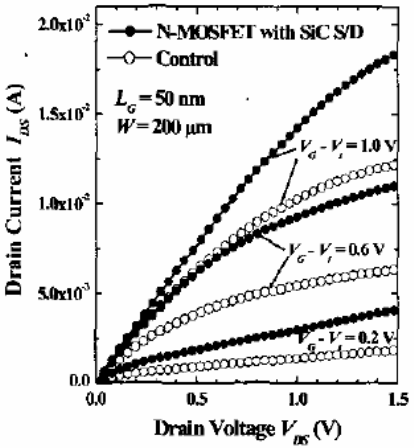
Chidambaram
TI / Applied Materials
VLSI - 2004

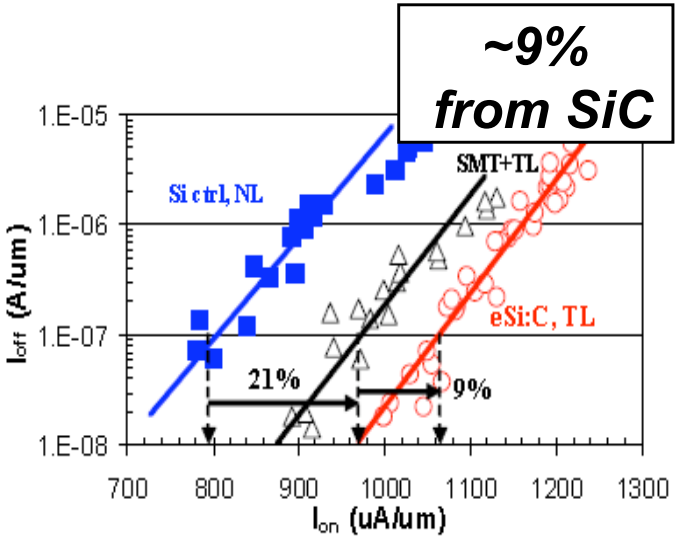
Embedded Si:C (NMOS)

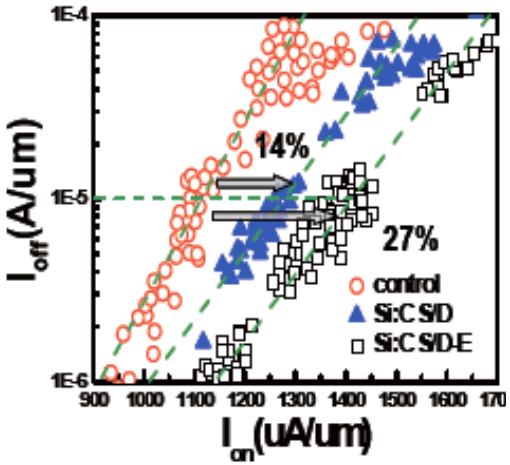










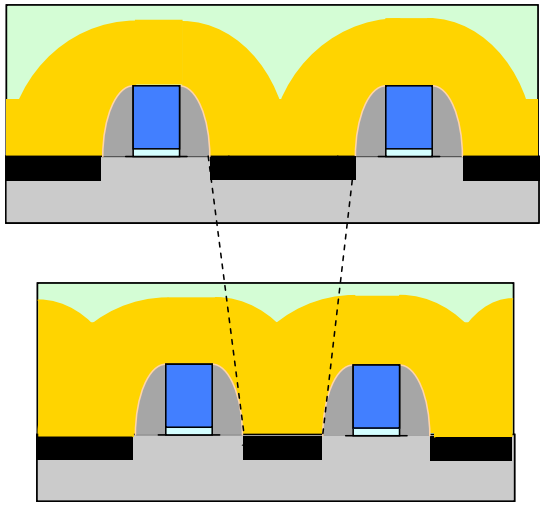


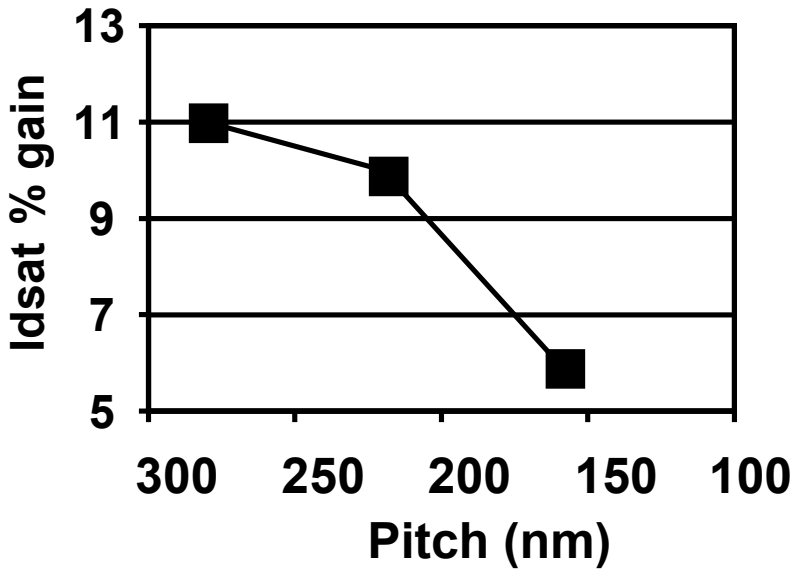
Ang – NUS-Singapore
IEDM 2004
Selective epi SiC (undoped)

Yang – IBM
IEDM 2008
In-situ epi P-SiC

Chung – Nat'l Chiao Tung U.
VLSI 2009
Implanted C + SPE

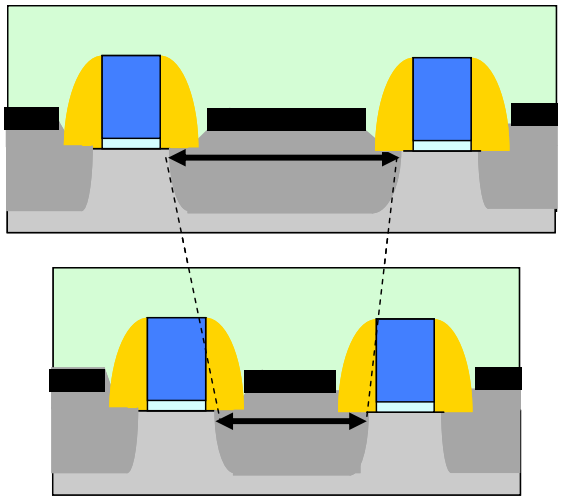
Strain: Pitch dependence

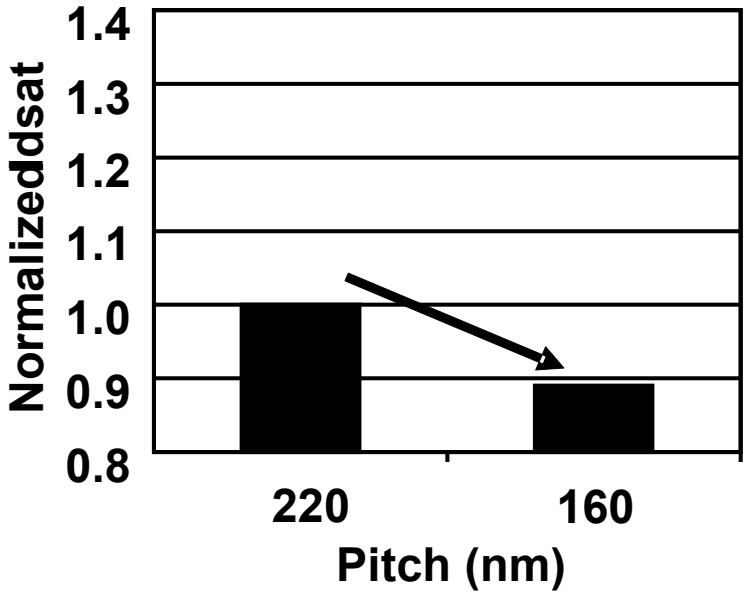




NMOS

Pitch degradation increases with film pinchoff, requires higher stress, thinner films





PMOS

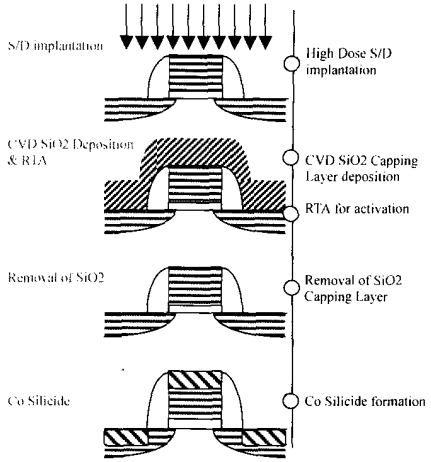
eSiGe S/D mobility strongly dependent on pitch

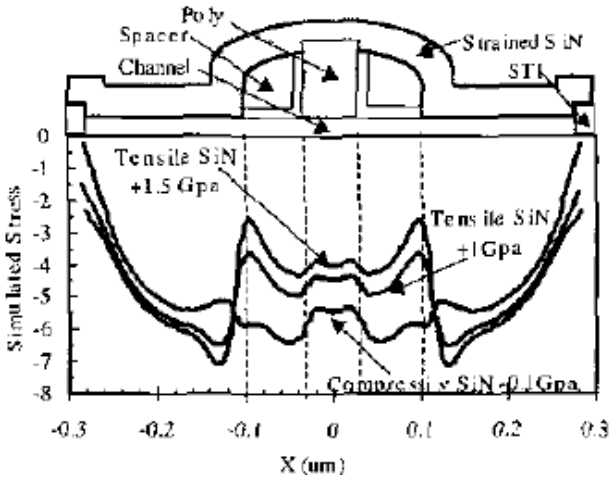
Auth, Intel, VLSI 2008

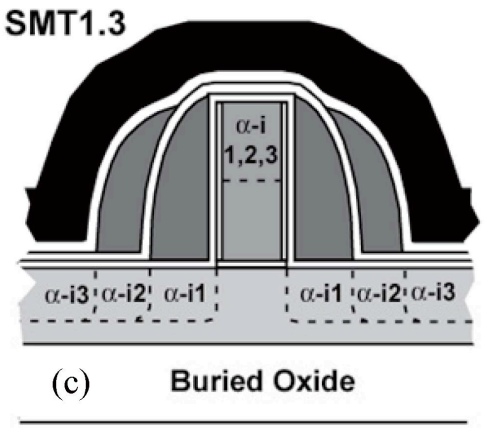
Strain: Pitch dependence

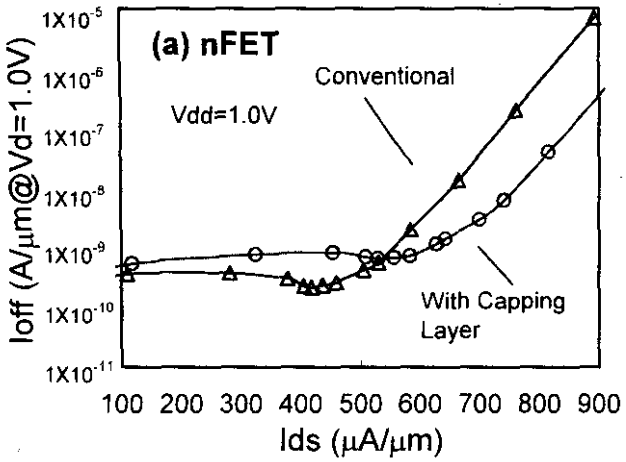
What about strain options less sensitive to pitch?

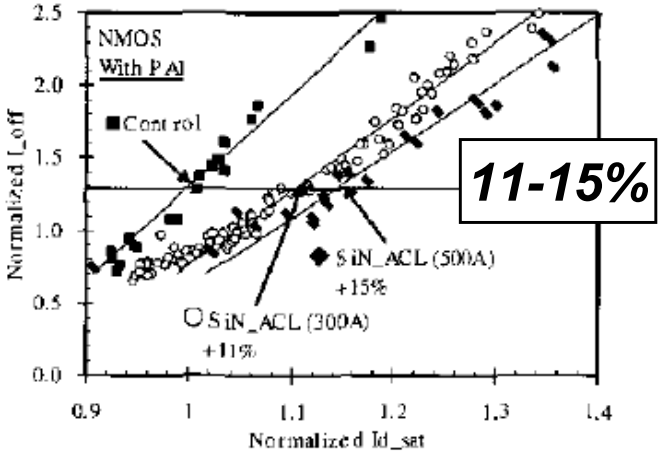
Stress Memorization (SMT)

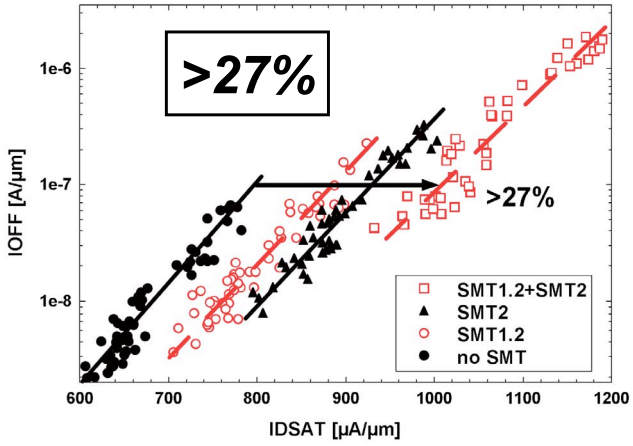










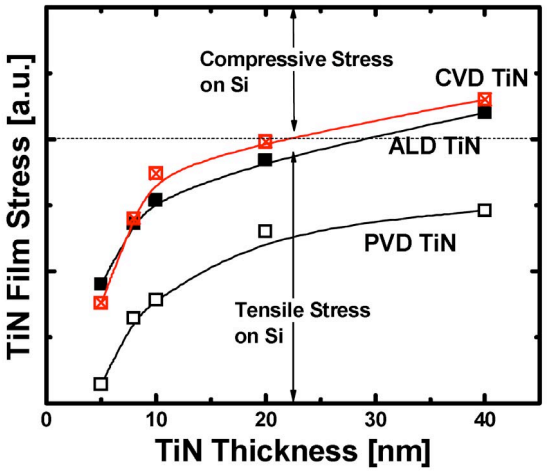


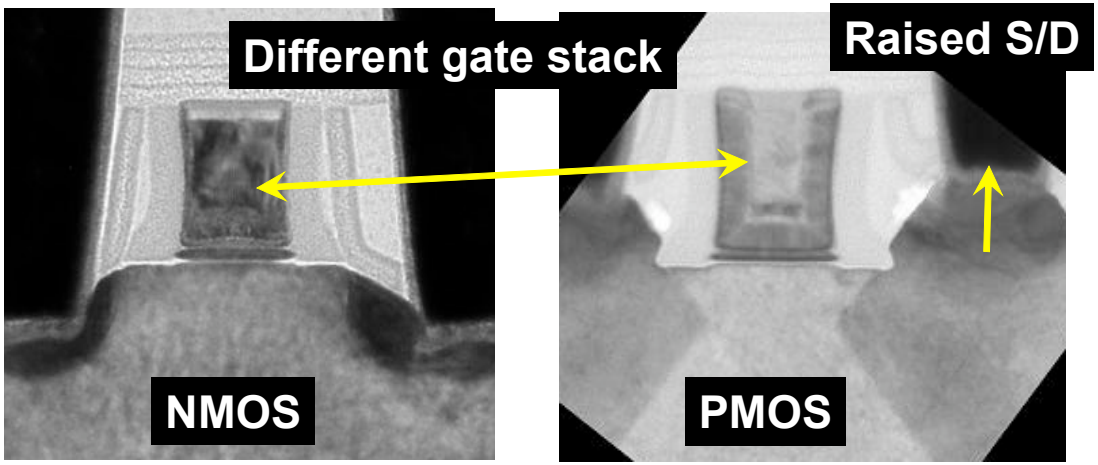
Ota – Mitsubishi
IEDM 2002
NMOS SMT

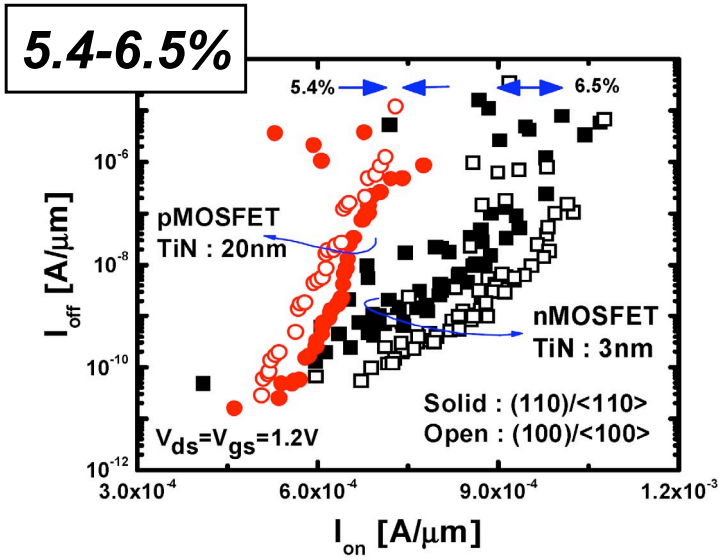
Chen – TSMC
VLSI 2004
NMOS SMT

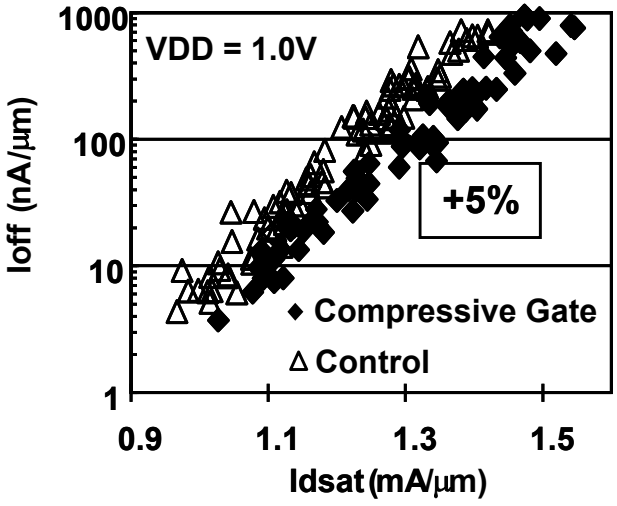
Wei – AMD
VLSI 2007
Multiple liners

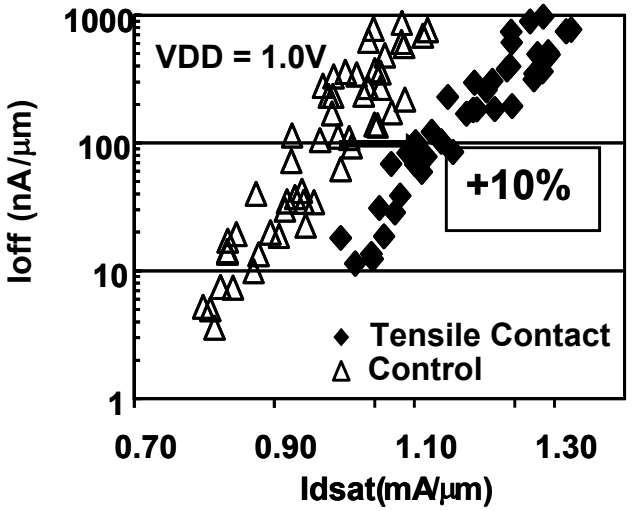
Metal stress (gate and contact)







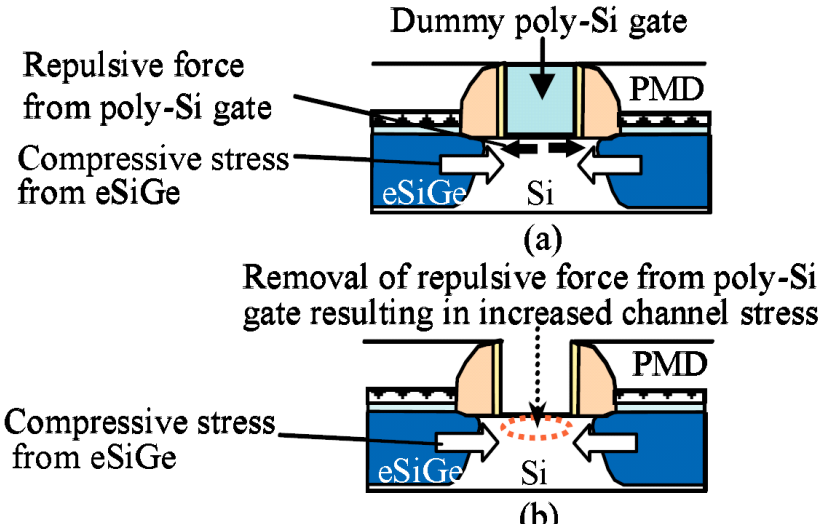




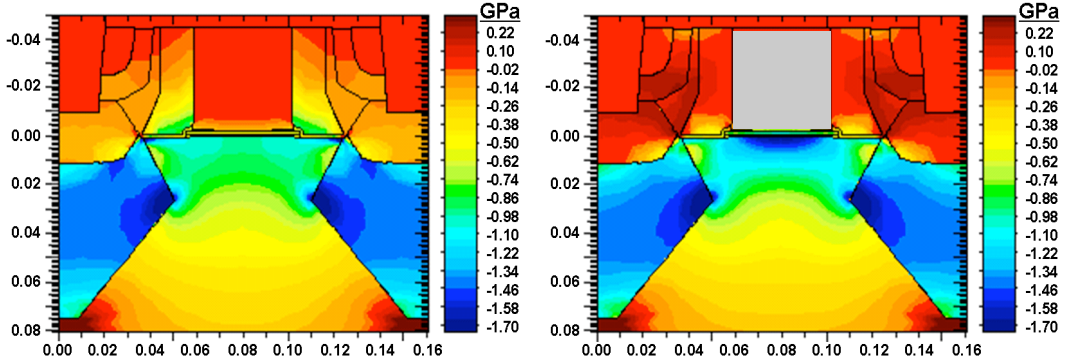
Kang – Sematech
IEDM 2006

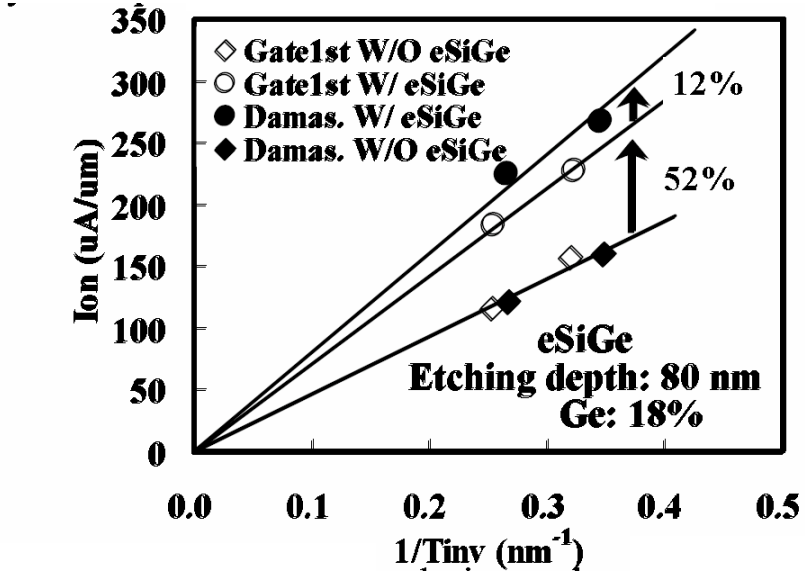
Auth – Intel
VLSI 2008

Enhanced PMOS strain: Gate last HiK-MG

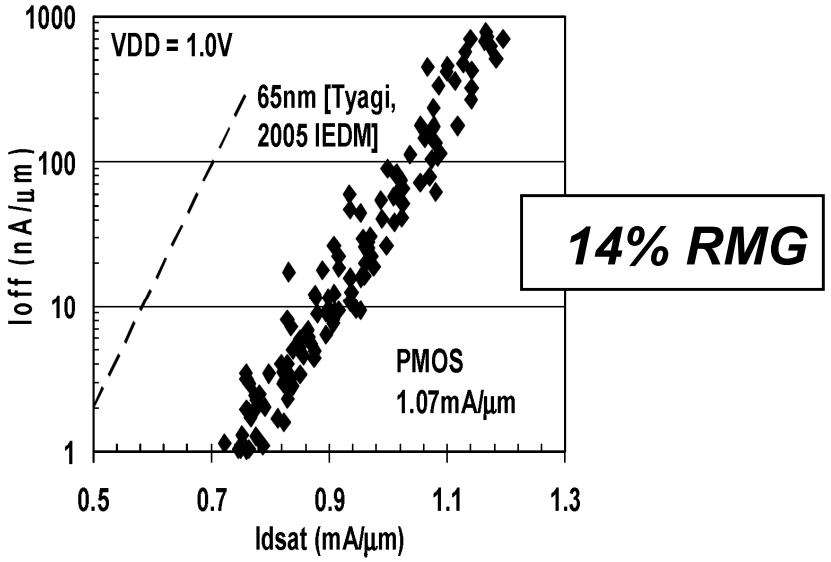


Before gate removal **After gate removal**





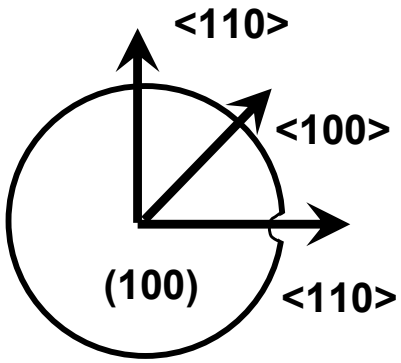
Wang – Sony
VLSI 2007



Auth – Intel
VLSI 2008

ORIENTATION

(100) surface – top down

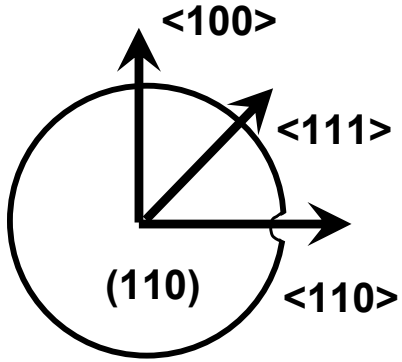


Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a “45 degree” wafer)

Both <110> directions are the same.

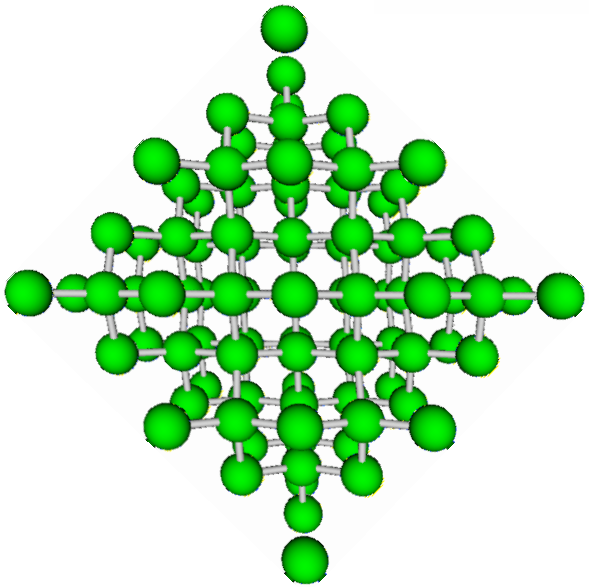
(110) surface – top down

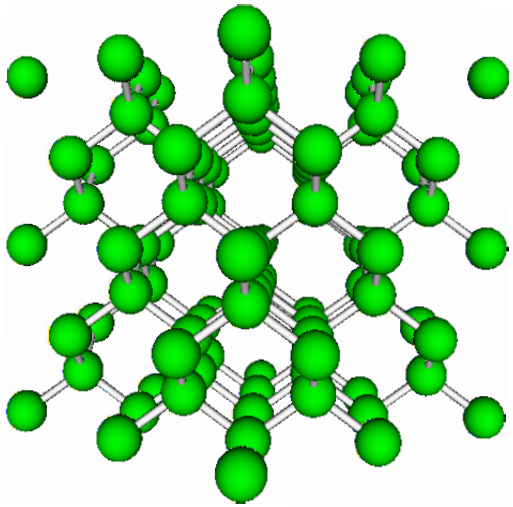


Non-standard

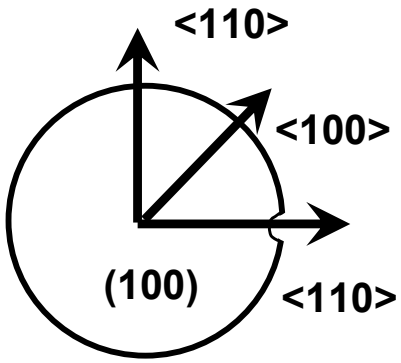
(110) Surface

Three possible channel directions
<110> <111> and <100>





(100) surface – top down

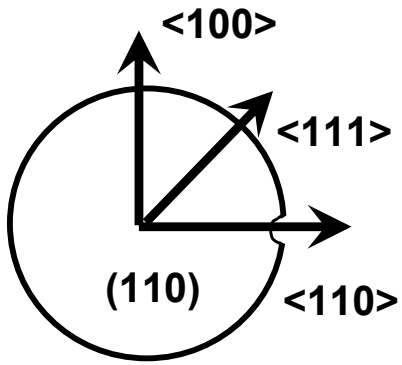


Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a "45 degree" wafer)

Both <110> directions are the same.

(110) surface – top down

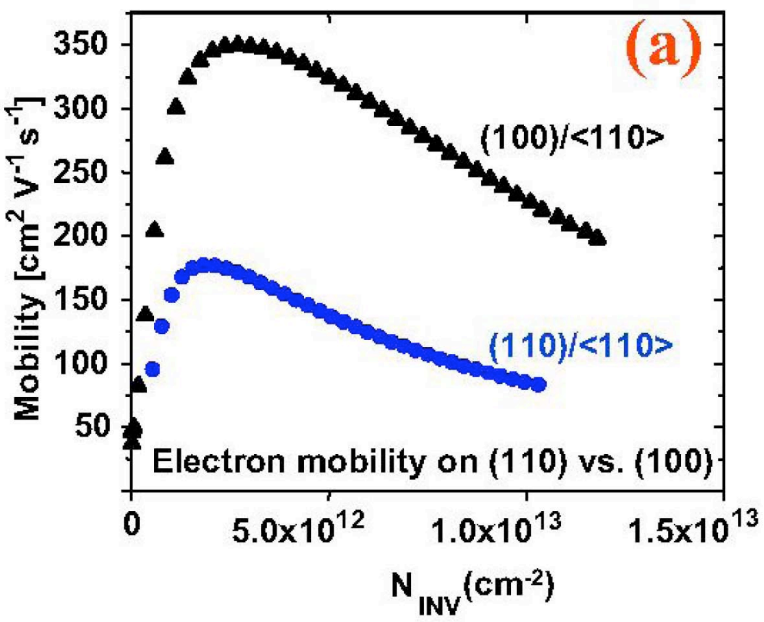


Non-standard

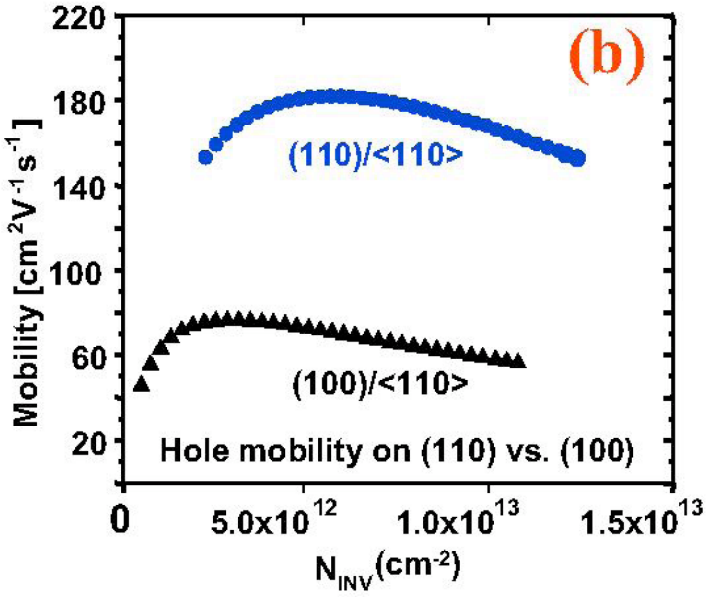
(110) Surface

Three possible channel directions
<110> <111> and <100>

(100) BEST NMOS

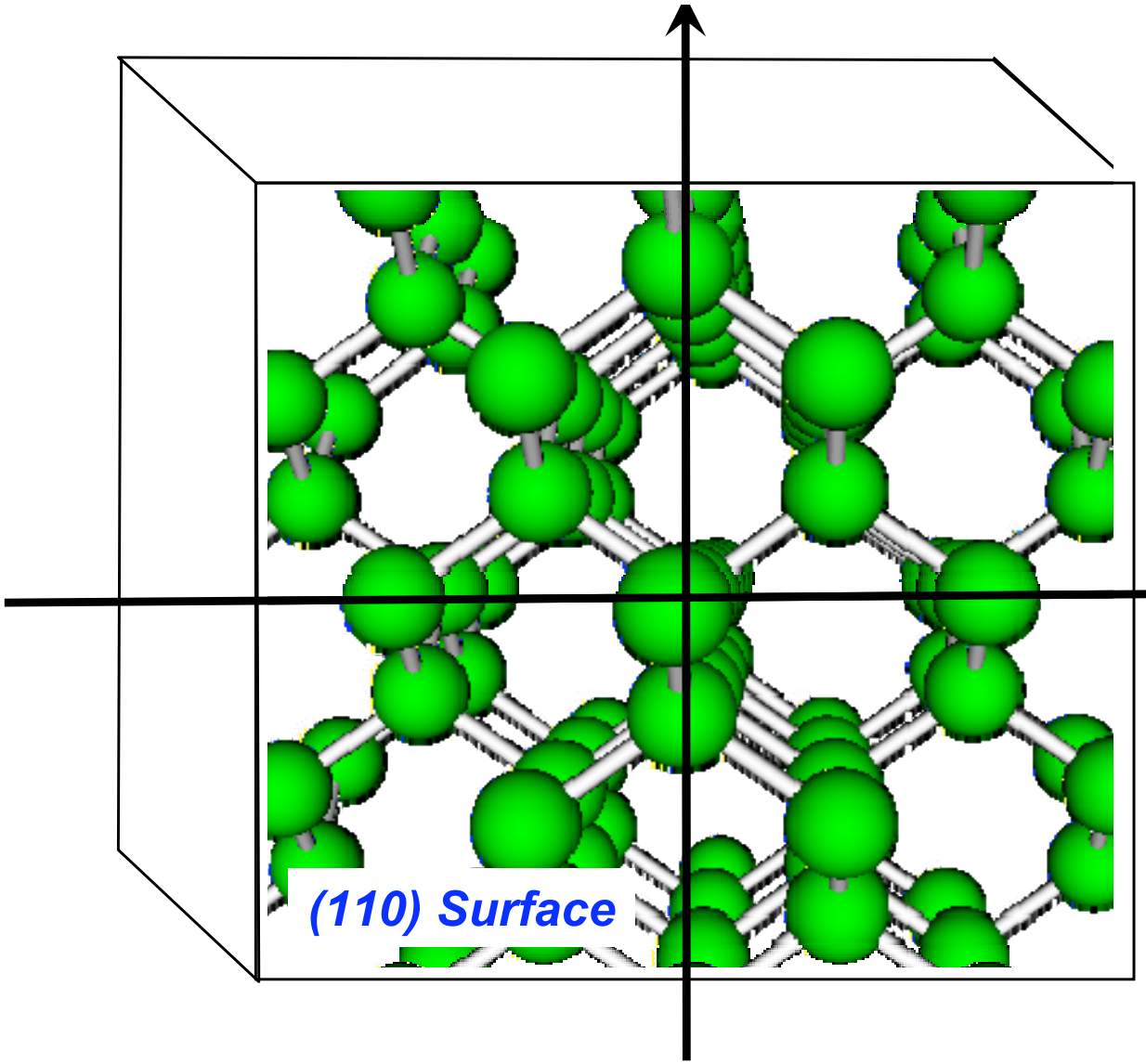


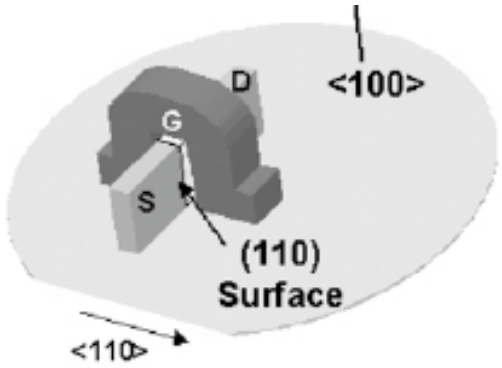
(110) <110> BEST PMOS



Yang
AMD/IBM
EDST 2007

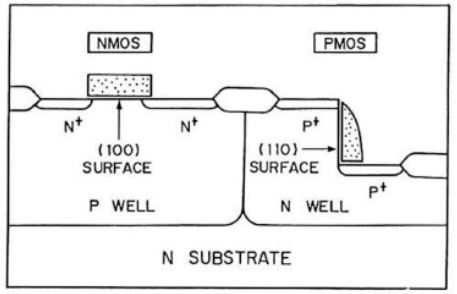
PMOS Vertical Devices on (100)





Chang - IBM – TED 2004

<110> channel

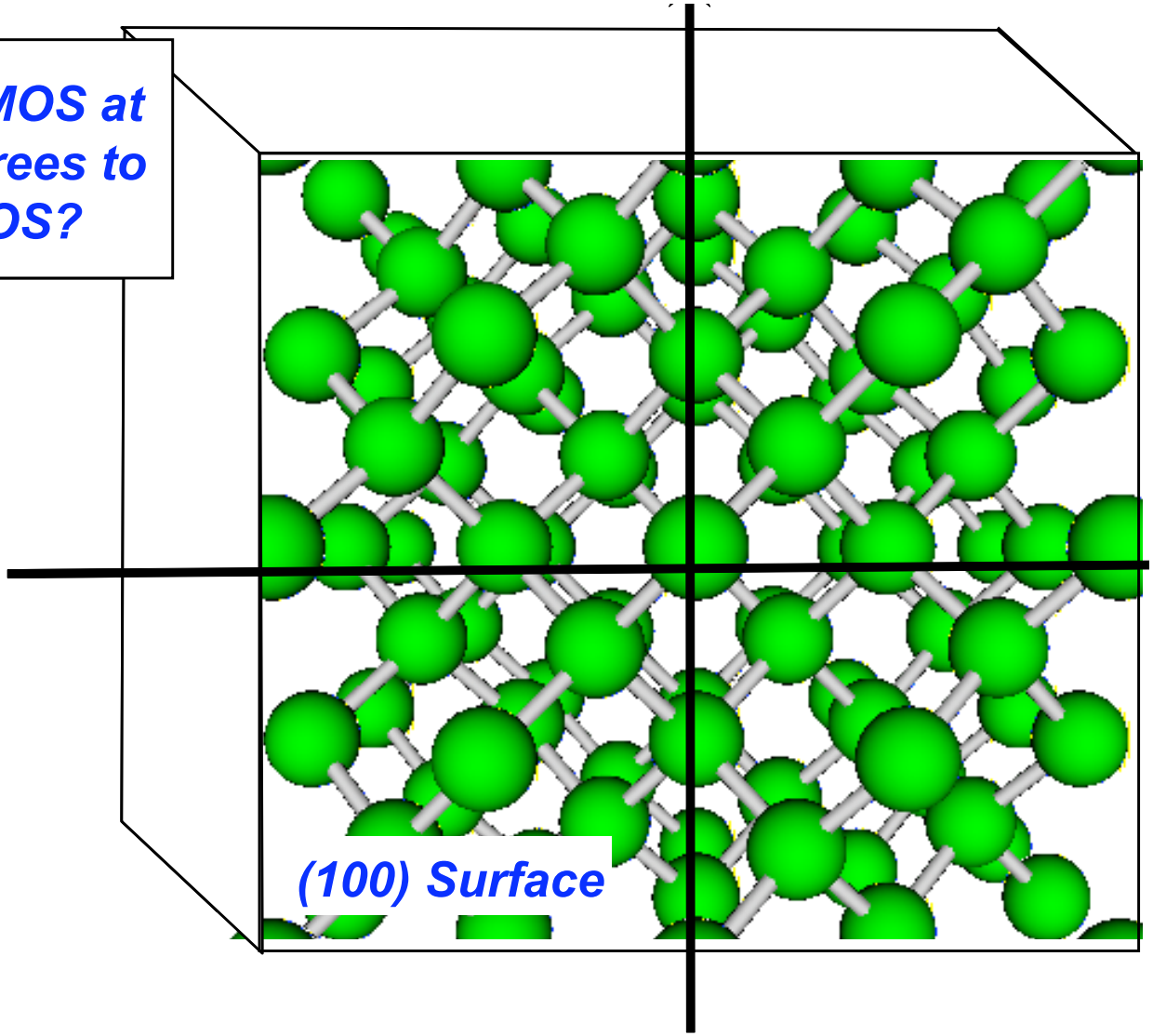


Kinugawa-Toshiba VLSI 1986

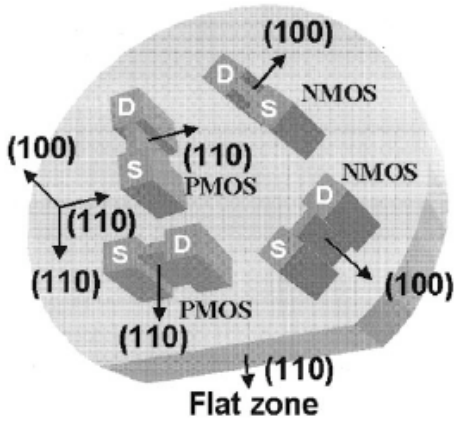
(110) surface <110> channel results when a VFET is fabricated on typical (100) Si - good for PMOS, not for NMOS

NMOS Vertical Devices on (100)

Put NMOS at 45degrees to PMOS?



<100> channel



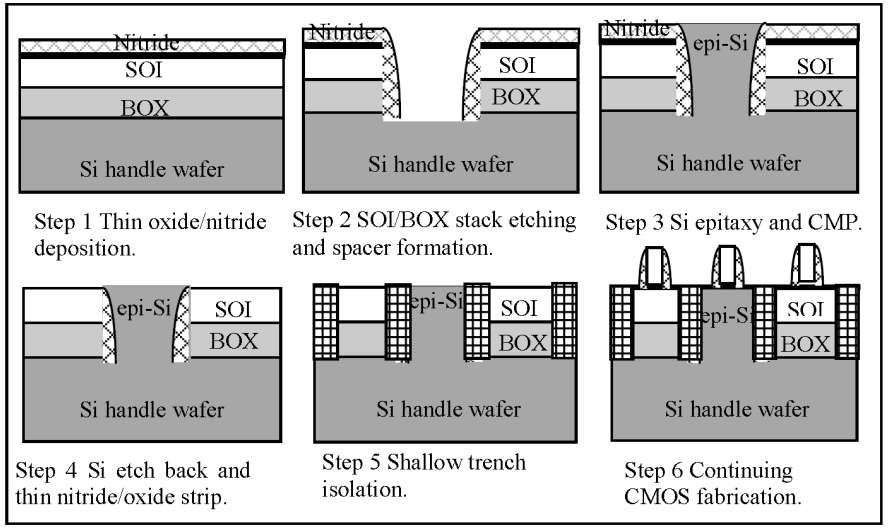
Chang - Berkeley
Proc. IEEE 2003

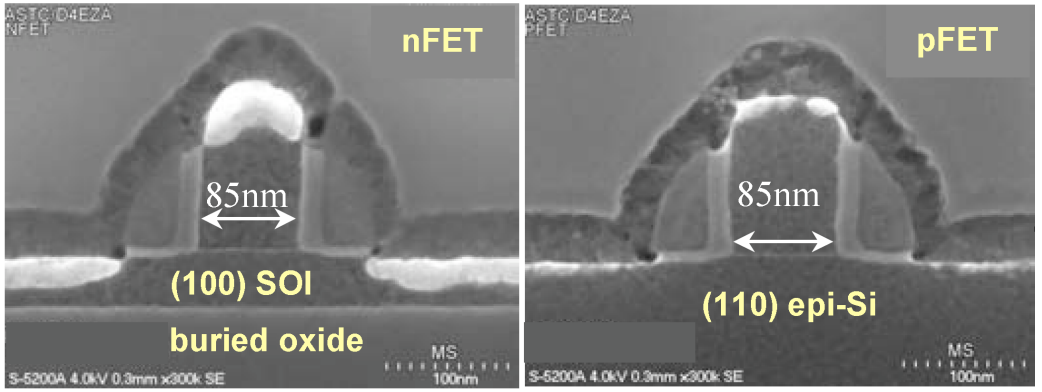
(100) surface <100> channel for a VFET fabricated at 45 degrees typical (100) Si – very challenging for lithography

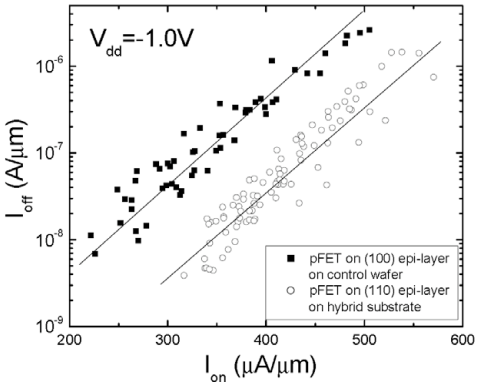
Wafer bonding; SOI of opposite type of handle wafer; both options (N and PMOS SOI explored)

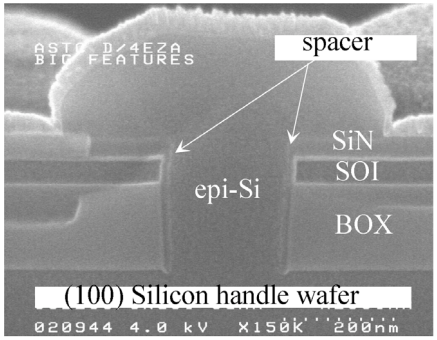
Early HOT

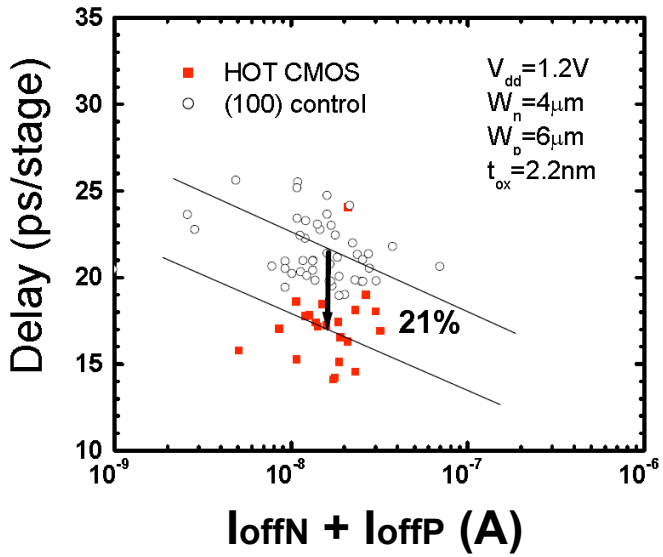
Elegant solution!







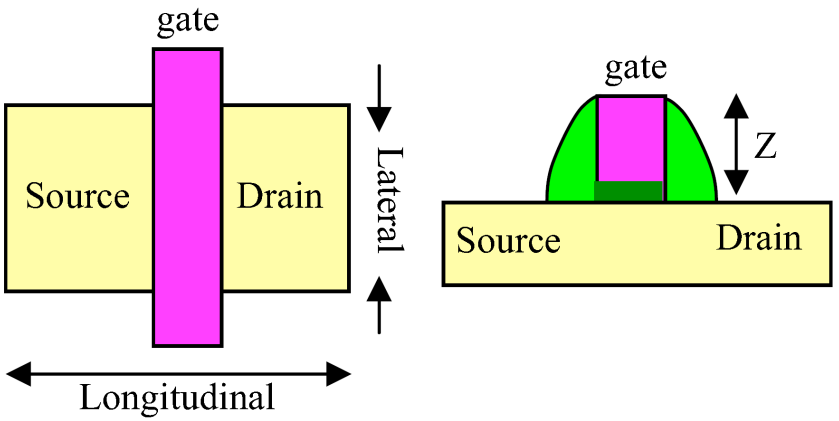




Yang – IBM
IEDM 2003 [28]
First HOT

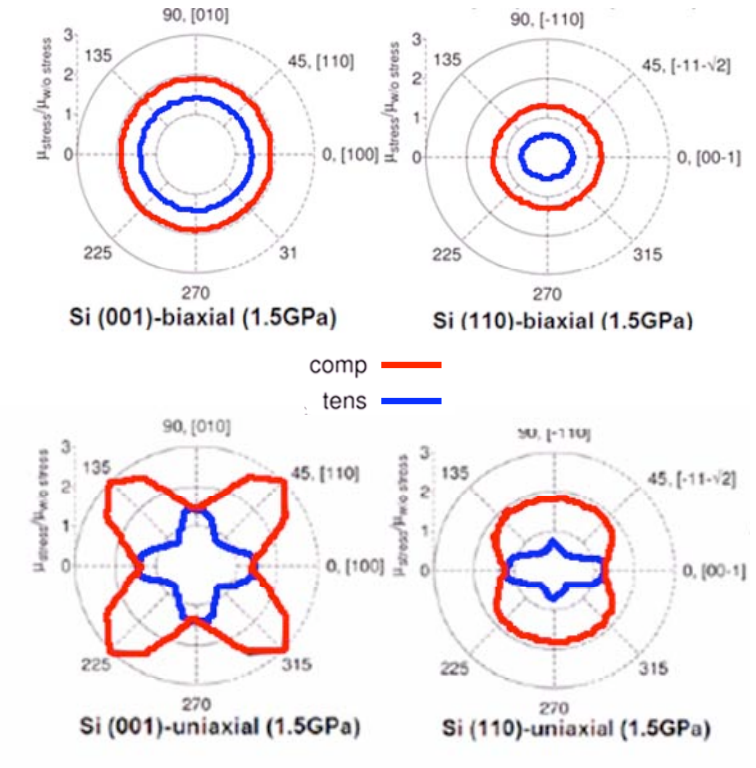
Yang – AMD/IBM
VLSI 2004
HOT RO

Strain AND orientation optimization



		NMOS	PMOS
Longitudinal	X	Tensile	Compressive
Lateral	Y	Tensile	Tensile
Si Depth	Z	Compressive	Tensile

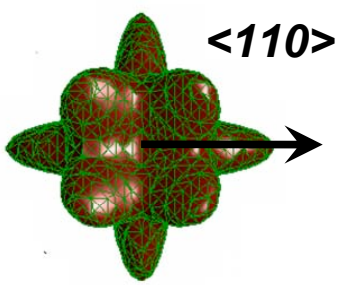
Chan – IBM
CICC 2005



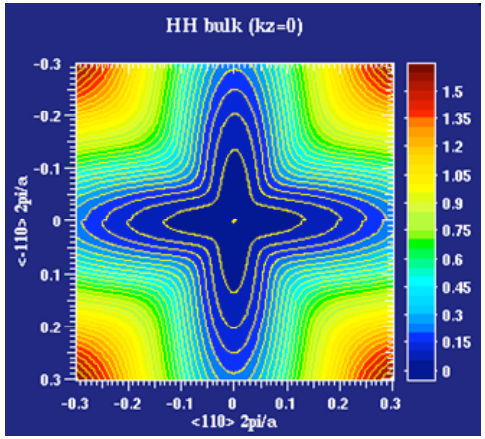
Krishnamohan – Stanford
IEDM 2008

More complex for non-(100) orientations

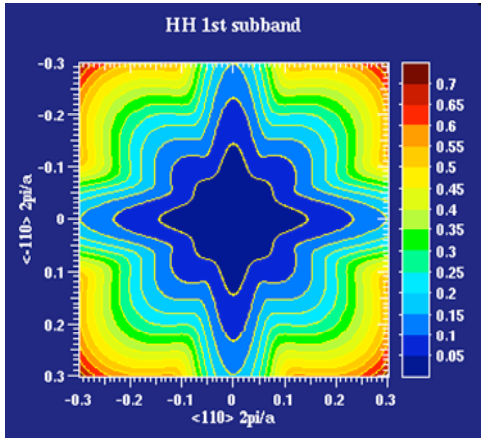
(100)



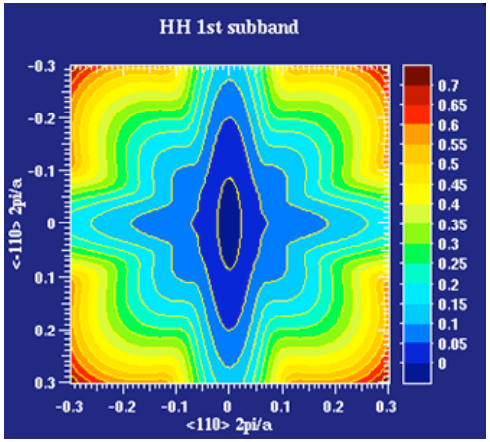
(001) Surface (k⊥=0)



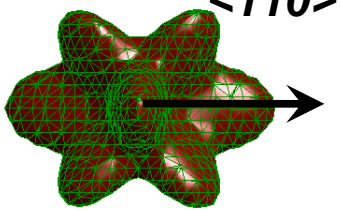
(001) Surface Vg=-1V



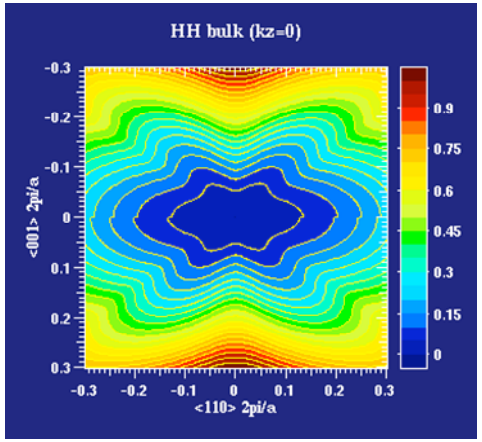
(001) Surface Vg=-1V, Sxx=-1GPa



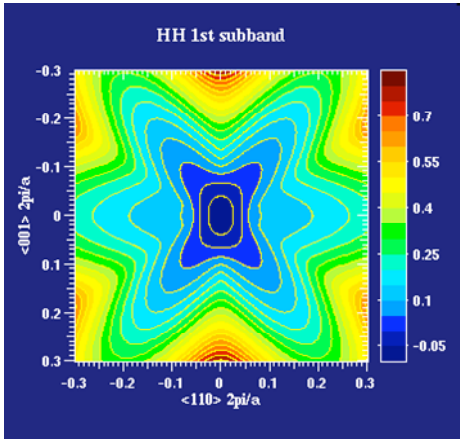
(110)



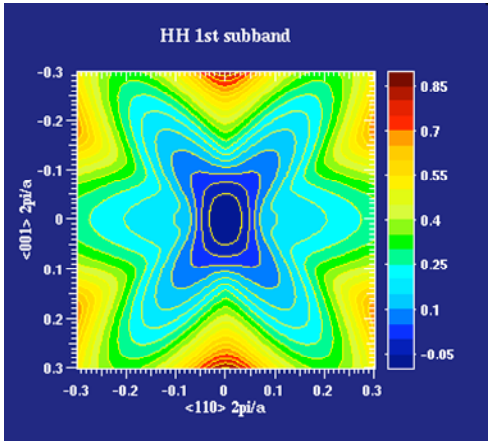
(110) Surface (k⊥=0)



(110) Surface Vg=-1V



(110) Surface Vg=-1V, Sxx=-1GPa



BULK **1'D CONFINED** **1'D CONFINED STRAINED**

AGENDA

- Scaling history
- Gate control
  - High-k metal-gate
  - Structural enhancements
- Resistance
- Capacitance
- Mobility
  - Strain
  - Orientation
- Summary

Looking Forward

Low risk

Further enhancements in strain technology
Further enhancements in HiK-MG technology

Medium Risk

Optimized substrate and channel orientation
Reduction in MOS parasitic resistance
Reduction in MOS parasitic capacitance

High risk

UTB devices
MuGFETS
Nanowires
Metal S/D devices


Questions???